4.5-V TO 52-V INPUT CURRENT MODE BOOST CONTROLLER

FEATURES

- For Boost, Flyback, SEPIC, LED Drive Apps
- Wide Input Operating Voltage: 4.5 V to 52 V
- Adjustable Oscillator Frequency
- Fixed Frequency Current Mode Control
- Internal Slope Compensation
- Integrated Low-Side Driver
- Programmable Closed Loop Soft Start
- Overcurrent Protection
- External Synchronization Capable
- Reference700-mV (TPS40210), 260-mV (TPS40211)
- Low Current Disable Function

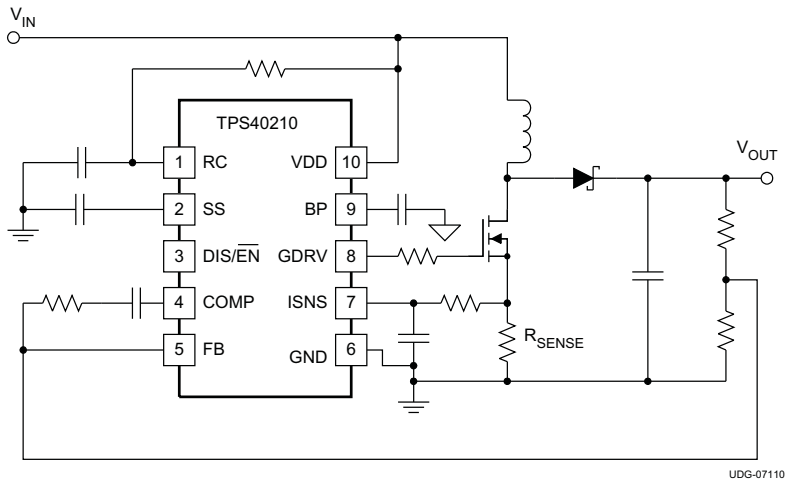
APPLICATIONS

- LED Lighting
- Industrial Control Systems
- Battery Powered Systems

CONTENTS

DESCRIPTION

The TPS40210 and TPS40211 are wide-input voltage (4.5 V to 52 V), non-synchronous boost controllers. They are suitable for topologies which require a grounded source N-channel FET including boost, flyback, SEPIC and various LED Driver applications. The device features include programmable soft start, overcurrent protection with automatic retry and programmable oscillator frequency. Current mode control provides improved transient response and simplified loop compensation. The main difference between the two parts is the reference voltage to which the error amplifier regulates the FB pin.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	PACKAGE	PACKAGE LEAD	TAPE AND REEL QUANTITY	PART NUMBER
-40°C to 125°C	10-Pin MSOP PowerPAD	DGQ	2500	TPS40210DGQR
			80	TPS40210DGQ
	10-Pin SON	DRC	3000	TPS40210DRCR
			250	TPS40210DRCT
-40°C to 125°C	10-Pin MSOP PowerPAD	DGQ	2500	TPS40211DGQR
			80	TPS40211DGQ
	10-Pin SON	DRC	3000	TPS40211DRCR
			250	TPS40211DRCT

DEVICE RATINGS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			TPS40210 TPS40211	UNIT
	Input voltage range	VDD	–0.3 to 52	V
		RC, SS, FB, DIS/$\overline{EN}$	–0.3 to 10	
		ISNS	–0.3 to 8	
	Output voltage range	COMP, BP, GDRV	–0.3 to 9	
T_J	Operating junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature		–55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{VDD}	Input voltage	4.5		52	V
T_J	Operating Junction temperature	-40		125	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	AIRFLOW (LFM)	$R_{\theta JA}$ High-K Board(1) (°C/W)	Power Rating (W) T_A = 25°C	Power Rating (W) T_A = 85°C
10-Pin MSOP PowerPAD (DGQ)	0 (Natural Convection)	57.7	1.73	0.693
10-Pin SON (DRC)	0 (Natural Convection)	47.9	2.08	0.835

(1) Ratings based on JEDEC High Thermal Conductivity (High K) Board. For more information on the test method, see TI Technical Brief SZZA017.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	TYP	MAX	UNIT
Human Body Model (HBM)		1500		V
Charged Device Model (CDM)		1500		

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_{VDD}= 12 V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE							
V_{FB}	Feedback voltage range	TPS40210	COMP = FB, 4.5 ≤ V_{VDD} ≤ 52 V, T_J = 25°C	693	700	707	mV
		TPS40211	COMP=FB, 4.5 ≤ V_{VDD} ≤ 52 V, T_J = 25°C	254	260	266	
		TPS40210	COMP = FB, 4.5 ≤ V_{VDD} ≤ 52 V, -40°C ≤ T_J ≤ 125°C	686	700	714	
		TPS40211	COMP = FB, 4.5 ≤ V_{VDD} ≤ 52 V, -40°C ≤ T_J ≤ 125°C	250	260	270	
INPUT SUPPLY							
V_{VDD}	Input voltage range			4.5		52	V
I_{VDD}	Operating current		4.5 ≤ V_{VDD} ≤ 52 V, no switching, V_{DIS} < 0.8		1.5	2.5	mA
			2.5 ≤ V_{DIS} ≤ 7 V		10	20	µA
			V_{VDD} < $V_{UVLO(on)}$, V_{DIS} < 0.8			530	µA
UNDERVOLTAGE LOCKOUT							
$V_{UVLO(on)}$	Turn on threshold voltage			4.00	4.25	4.50	V
$V_{UVLO(hyst)}$	UVLO hysteresis			140	195	240	mV
OSCILLATOR							
f_{OSC}	Oscillator frequency range(1)			35		1000	kHz
	Oscillator frequency		R_{RC} = 182 kΩ, C_{RC} = 330 pF	260	300	340	
	Frequency line regulation		4.5 ≤ V_{DD} ≤ 52 V	-20%		7%	
V_{SLP}	Slope compensation ramp			520	620	720	mV
PWM							
$t_{ON(min)}$	Minimum pulse width		V_{VDD} = 12V(1)		275	400	ns
			V_{VDD} = 30V		90	200	
$t_{OFF(min)}$	Minimum off time				170	200	
V_{VLY}	Valley voltage				1.2		V
SOFT-START							
$V_{SS(ofst)}$	Offset voltage from SS pin to error amplifier input				700		mV
$R_{SS(chg)}$	Soft-start charge resistance			320	430	600	kΩ
$R_{SS(dchg)}$	Soft-start discharge resistance			840	1200	1600	
ERROR AMPLIFIER							
GBWP	Unity gain bandwidth product(1)			1.5	3.0		MHz
A_{OL}	Open loop gain(1)			60	80		dB
$I_{IB(FB)}$	Input bias current (current out of FB pin)				100	300	nA
$I_{COMP(src)}$	Output source current		V_{FB} = 0.6 V, V_{COMP} = 1 V	100	250		µA
$I_{COMP(snk)}$	Output sink current		V_{FB} = 1.2 V, V_{COMP} = 1 V	1.2	2.5		mA
OVERCURRENT PROTECTION							
$V_{ISNS(oc)}$	Overcurrent detection threshold (at ISNS pin)		4.5 ≤ V_{DD} < 52 V, -40°C ≤ T_J ≤ 125°C	120	150	180	mV
D_{OC}	Overcurrent duty cycle(1)					2%	
$V_{SS(rst)}$	Overcurrent reset threshold voltage (at SS pin)			100	150	350	mV
T_{BLNK}	Leading edge blanking(1)				75		ns

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{VDD}= 12 V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE AMPLIFIER						
A_{CS}	Current sense amplifier gain		4..2	5.6	7.2	V/V
$I_{B(ISNS)}$	Input bias current			1	3	µA
DRIVER						
$I_{GDRV(src)}$	Gate driver source current	V_{GDRV} = 4 V, T_J = 25°C	375	400		mA
$I_{GDRV(snk)}$	Gate driver sink current	V_{GDRV} = 4 V, T_J = 25°C	330	400		
LINEAR REGULATOR						
V_{BP}	Bypass voltage output	0 mA < I_{BP} < 15 mA	7	8	9	V
DISABLE/ENABLE						
$V_{DIS(en)}$	Turn on voltage		0.7		1.3	V
$V_{DIS(hys)}$	Hysteresis voltage		25	130	220	mV
R_{DIS}	DIS pin pulldown resistance		0.7	1.1	1.5	MΩ

TYPICAL CHARACTERISTICS

FREQUENCY
vs
TIMING RESISTANCE

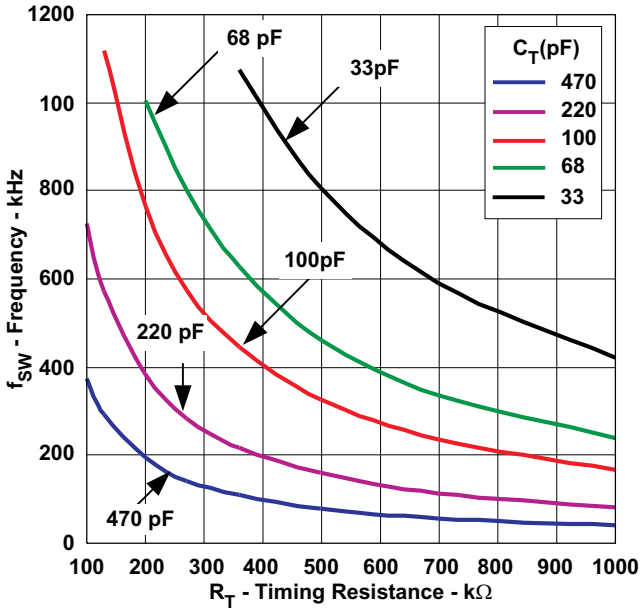


Figure 1.

SWITCHING FREQUENCY
vs
DUTY CYCLE

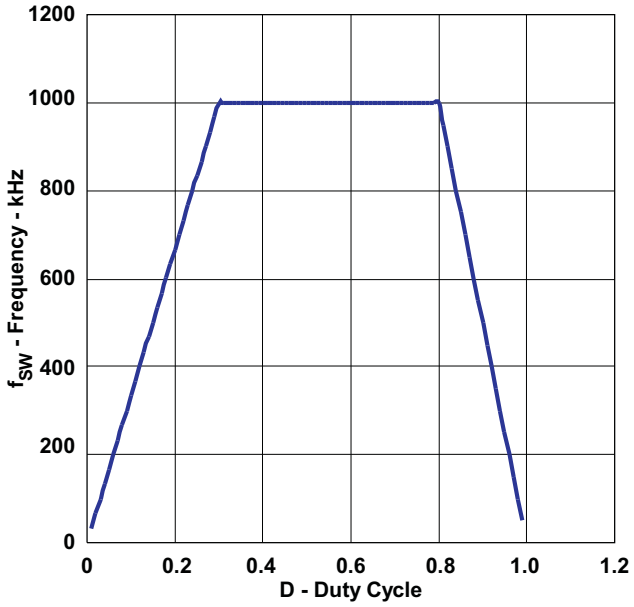


Figure 2.

QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

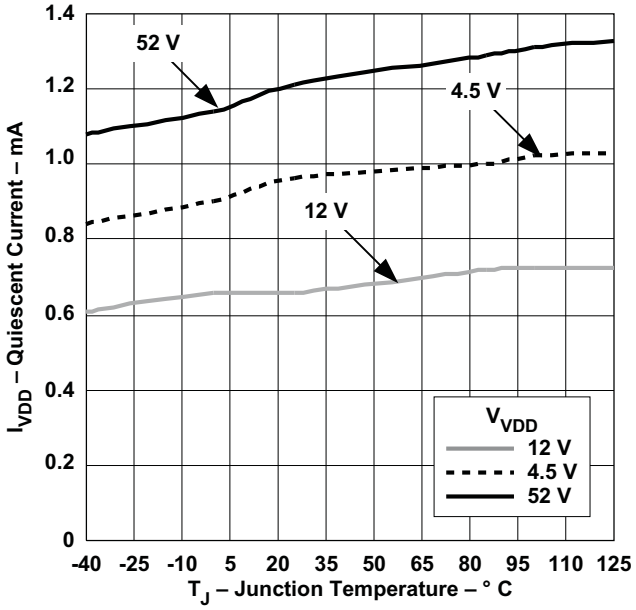


Figure 3.

SHUTDOWN CURRENT
vs
JUNCTION TEMPERATURE

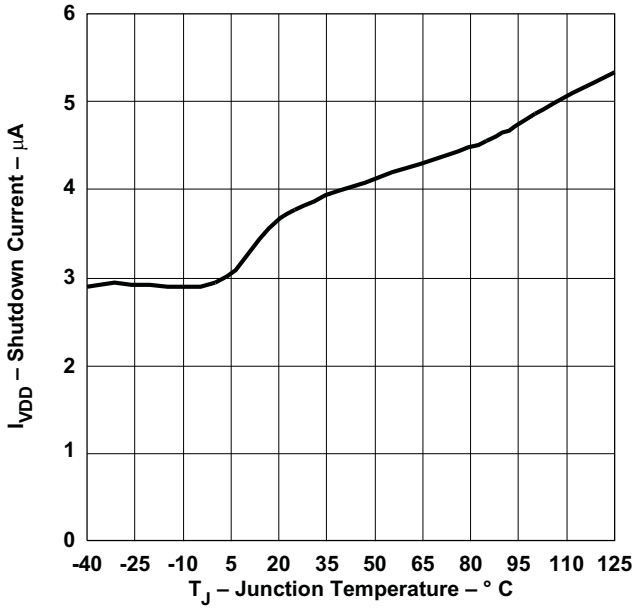


Figure 4.

TYPICAL CHARACTERISTICS (continued)

REFERENCE VOLTAGE CHANGE
vs
JUNCTION TEMPERATURE

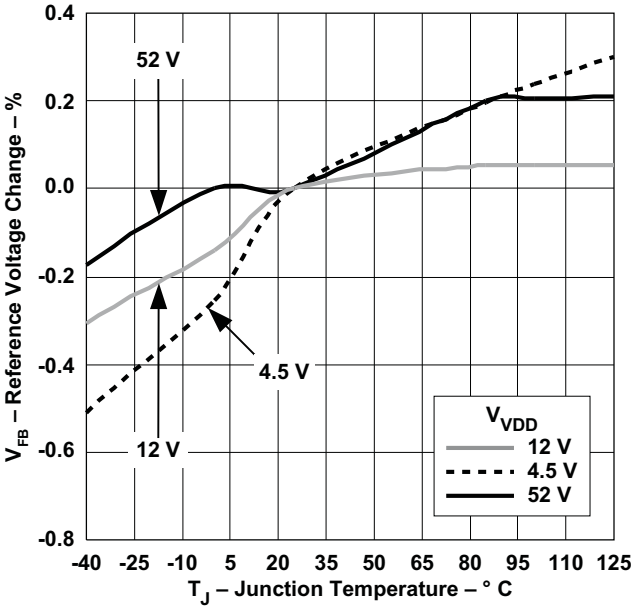


Figure 5.

REFERENCE VOLTAGE CHANGE
vs
INPUT VOLTAGE

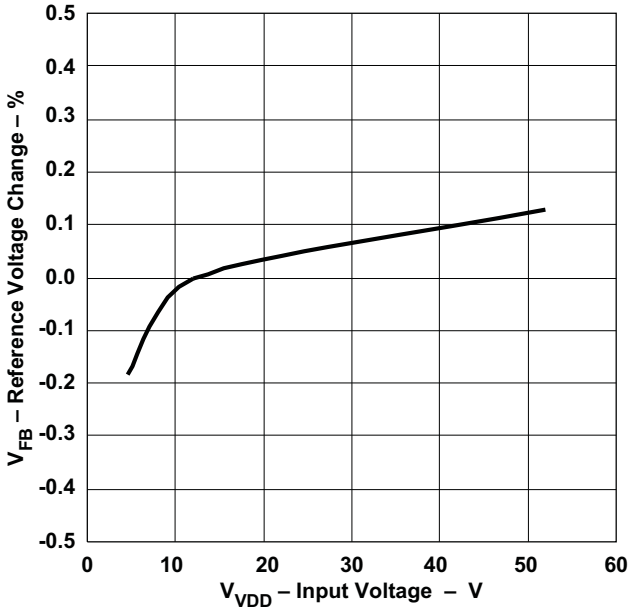


Figure 6.

UNDERVOLTAGE LOCKOUT THRESHOLD
vs
JUNCTION TEMPERATURE

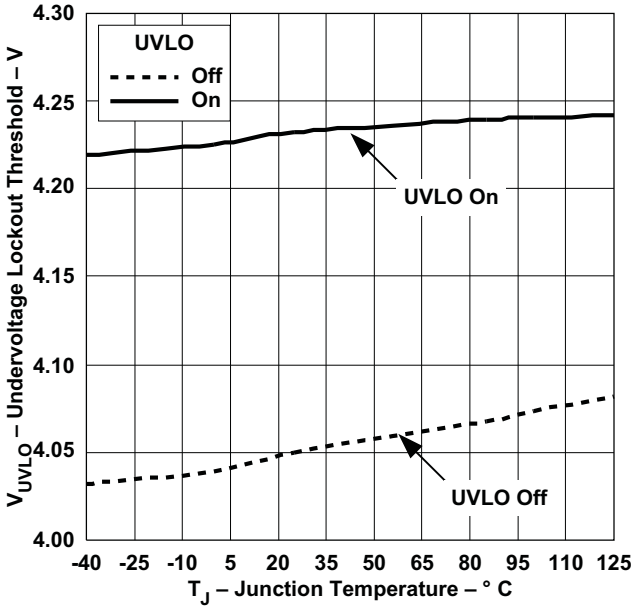


Figure 7.

OVERCURRENT THRESHOLD
vs
JUNCTION TEMPERATURE

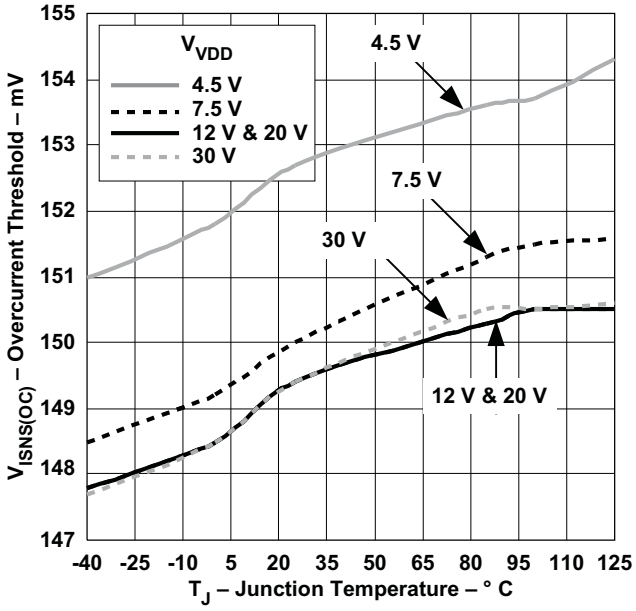


Figure 8.

TYPICAL CHARACTERISTICS (continued)

OVERCURRENT THRESHOLD vs INPUT VOLTAGE

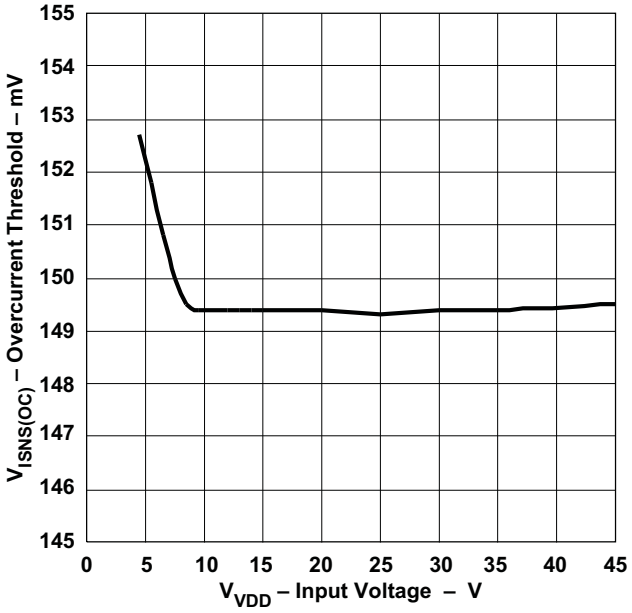


Figure 9.

SWITCHING FREQUENCY CHANGE vs JUNCTION TEMPERATURE

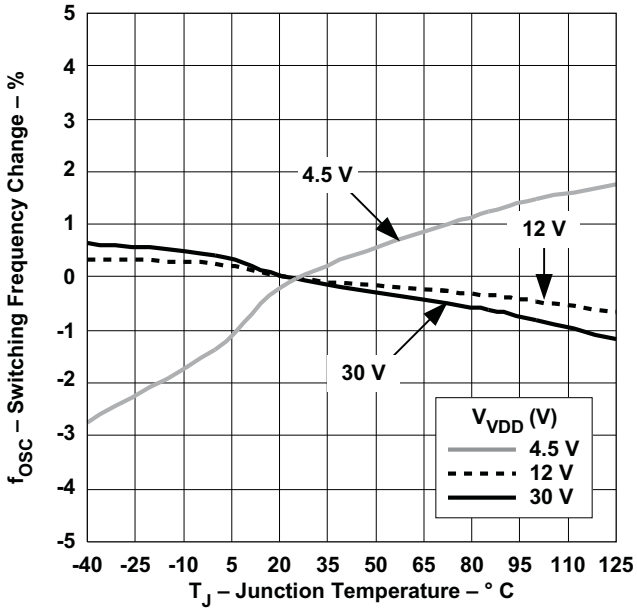


Figure 10.

OSCILLATOR AMPLITUDE vs JUNCTION TEMPERATURE

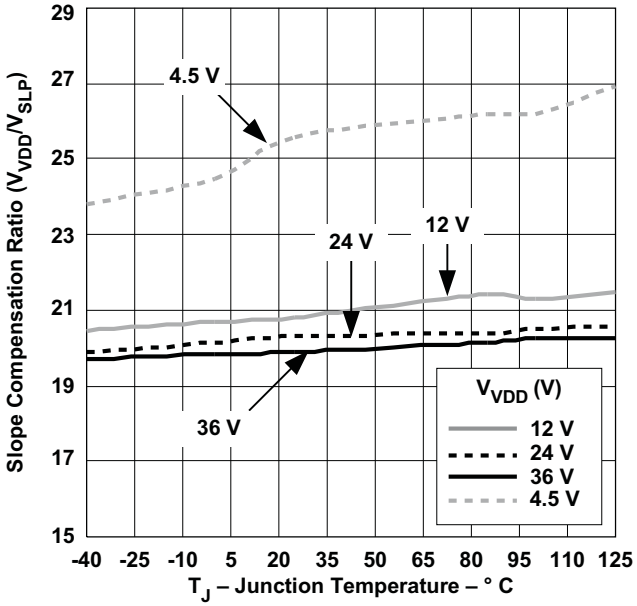


Figure 11.

SOFT-START CHARGE/DISCHARGE RESISTANCE vs JUNCTION TEMPERATURE

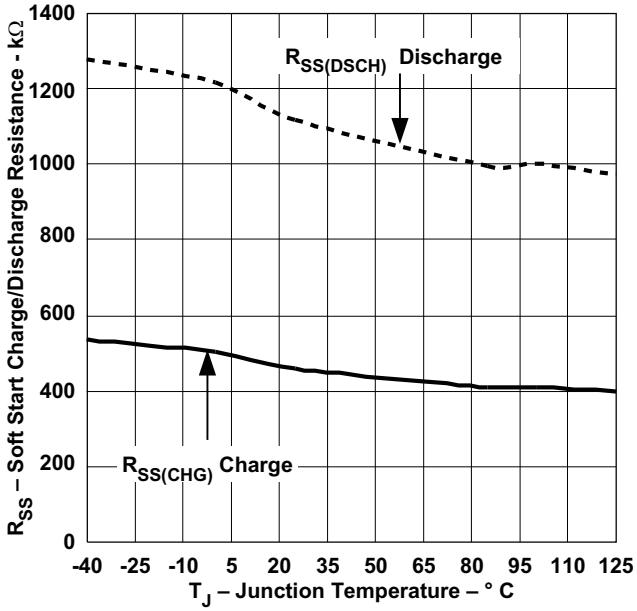


Figure 12.

TYPICAL CHARACTERISTICS (continued)

FB BIAS CURRENT vs JUNCTION TEMPERATURE

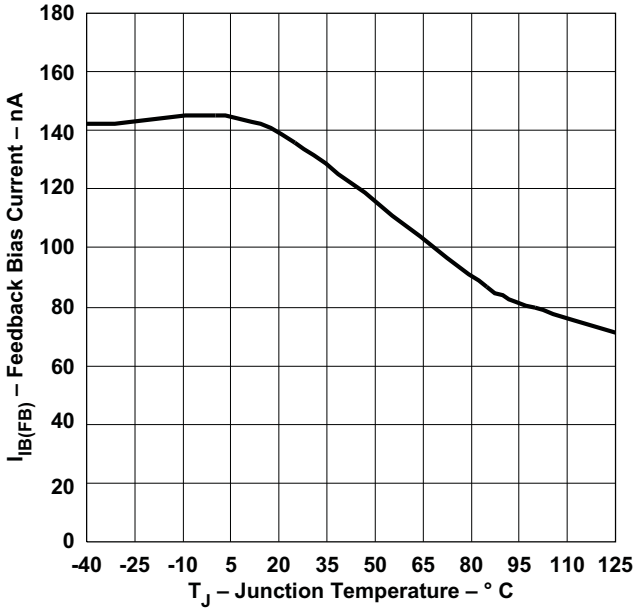


Figure 13.

COMPENSATION SOURCE CURRENT vs JUNCTION TEMPERATURE

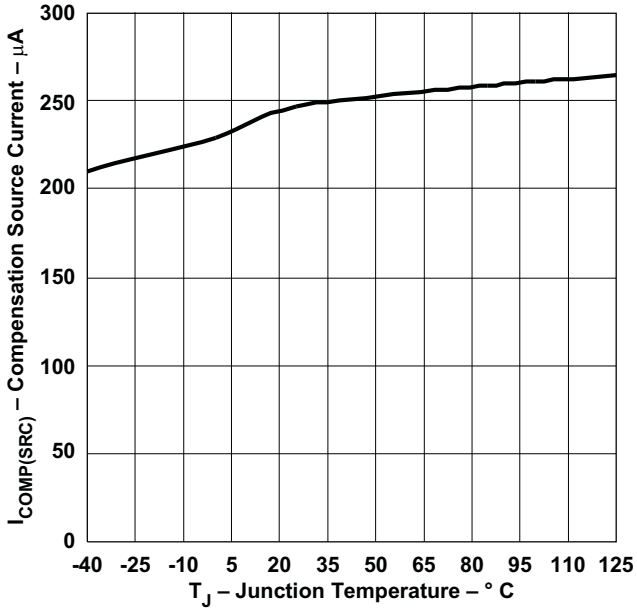


Figure 14.

COMPENSATION SINK CURRENT vs JUNCTION TEMPERATURE

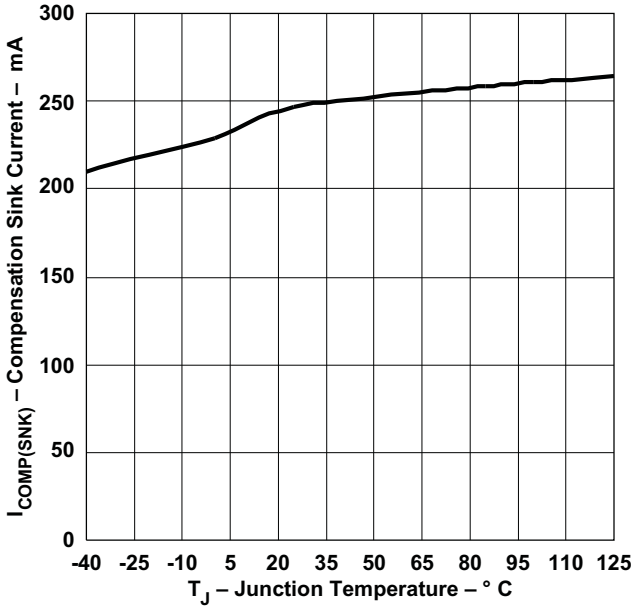


Figure 15.

VALLEY VOLTAGE CHANGE vs JUNCTION TEMPERATURE

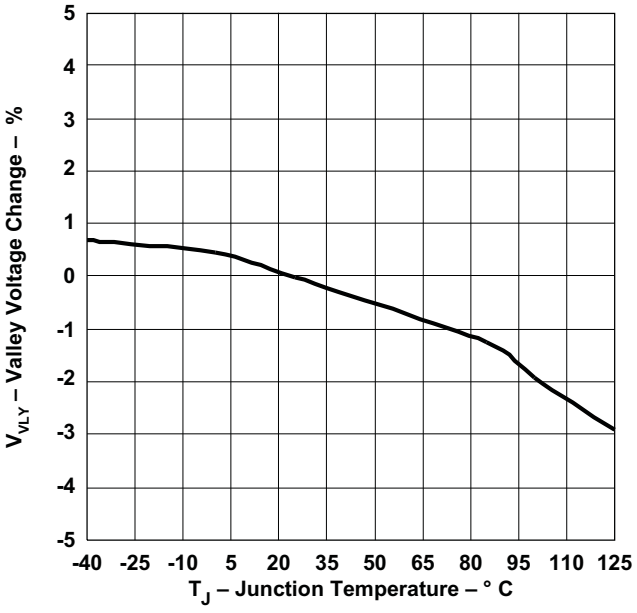


Figure 16.

TYPICAL CHARACTERISTICS (continued)

REGULATOR VOLTAGE vs JUNCTION TEMPERATURE

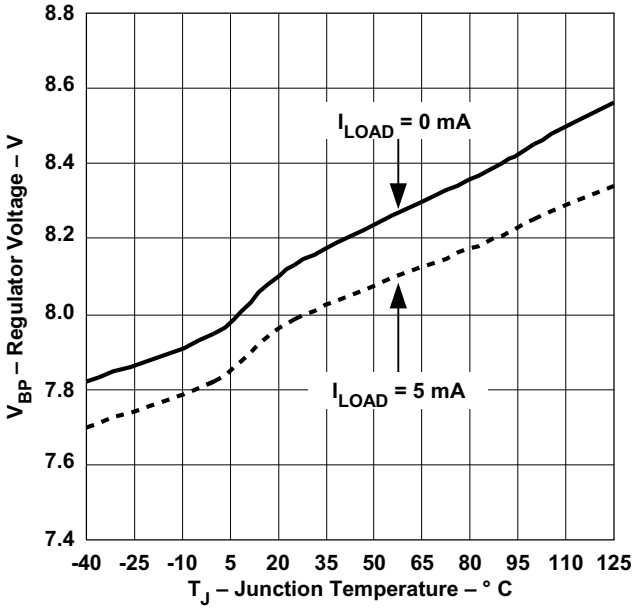


Figure 17.

DIS/$\overline{EN}$ TURN-ON THRESHOLD vs JUNCTION TEMPERATURE

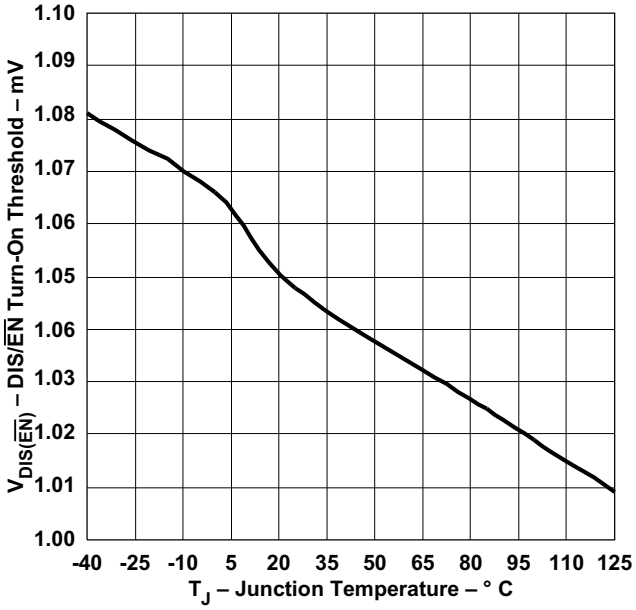


Figure 18.

CURRENT SENSE AMPLIFIER GAIN vs JUNCTION TEMPERATURE

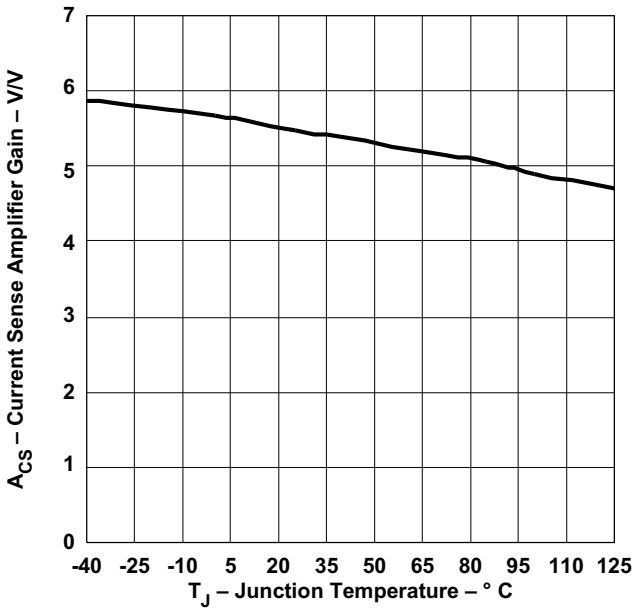


Figure 19.

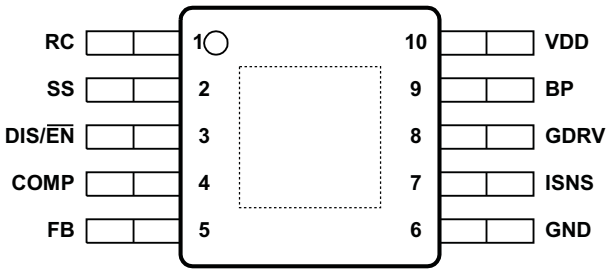
DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
COMP	4	O	Error amplifier output. Connect control loop compensation network between COMP pin and FB pin.
DIS/$\overline{EN}$	3	I	Disable pin. Pulling this pin high, places the part into a shutdown mode. Shutdown mode is characterized by a very low quiescent current. While in shutdown mode, the functionality of all blocks is disabled and the BP regulator is shut down. This pin has an internal 1-MΩ pull-down resistor to GND. Leaving this pin unconnected enables the device.
FB	5	I	Error amplifier inverting input. Connect a voltage divider from the output to this pin to set output voltage. Compensation network is connected between this pin and COMP.
GDRV	8	O	Connect the gate of the power N channel MOSFET to this pin.
GND	6	-	Device ground.
ISNS	7	I	Current sense pin. Connect an external current sensing resistor between this pin and GND. The voltage on this pin is used to provide current feedback in the control loop and detect an overcurrent condition. An overcurrent condition is declared when ISNS pin voltage exceeds the overcurrent threshold voltage, 150 mV typical.
RC	1	I	Switching frequency setting pin. Connect capacitor from RC pin to GND. Connect a resistor from RC pin toVDD of the IC power supply and a capacitor from RC to GND.
SS	2	I	Soft-start time programming pin. Connect capacitor from SS pin to GND to program converter soft-start time. This pin also functions as a timeout timer when the power supply is in an overcurrent condition.
BP	9	O	Regulator output pin. Connect a 1.0-µF bypass capacitor from this pin to GND.
VDD	10	I	System input voltage. Connect a local bypass capacitor from this pin to GND. Depending on the amount of required slope compensation, this pin can be connected to the converter output. See Application Information section for additional details.

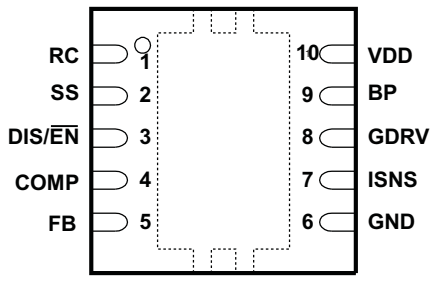
DGQ PowerPAD PACKAGE
(TOP VIEW)

DGQ PowerPAD PACKAGE
(Top View)

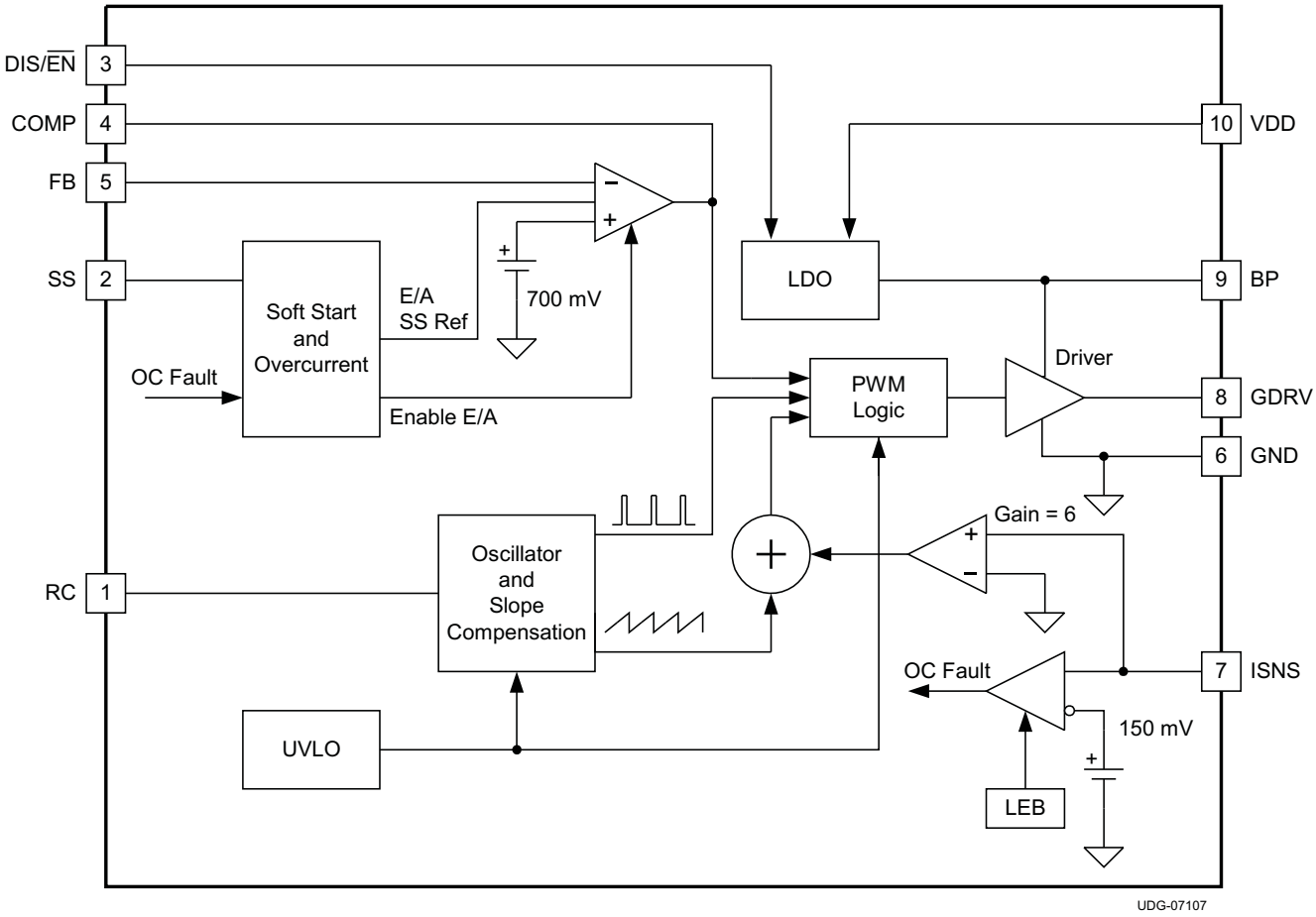


DRC PACKAGE
(TOP VIEW)

DRC SURFACE MOUNT PACKAGE
(Top View)



FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

Minimum On-Time and Off Time Considerations

The TPS40210 has a minimum off time of approximately 200 ns and a minimum on time of 300 ns. These two constraints place limitations on the operating frequency that can be used for a given input to output conversion ratio. See Figure 2 for the maximum frequency that can be used for a given duty cycle.

The duty cycle at which the converter operates is dependent on the mode in which the converter is running. If the converter is running in discontinuous conduction mode, the duty cycle varies with changes to the load much more than it does when running in continuous conduction mode.

In continuous conduction mode, the duty cycle is related primarily to the input and output voltages.

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{1}{1 - D} \tag{1}$$

$$D = \left(1 - \left(\frac{V_{IN}}{V_{OUT} + V_D}\right)\right) \tag{2}$$

In discontinuous mode the duty cycle is a function of the load, input and output voltages, inductance and switching frequency.

$$D = \frac{2 \times (V_{OUT} + V_D) \times I_{OUT} \times L \times f_{SW}}{(V_{IN})^2} \tag{3}$$

All converters using a diode as the freewheeling or catch component have a load current level at which they transition from discontinuous conduction to continuous conduction. This is the point where the inductor current just falls to zero. At higher load currents, the inductor current does not fall to zero but remains flowing in a positive direction and assumes a trapezoidal wave shape as opposed to a triangular wave shape. This load boundary between discontinuous conduction and continuous conduction can be found for a set of converter parameters as follows.

$$I_{OUT(crit)} = \frac{(V_{OUT} + V_D - V_{IN}) \times (V_{IN})^2}{2 \times (V_{OUT} + V_D)^2 \times f_{SW} \times L} \tag{4}$$

For loads higher than the result of Equation 4, the duty cycle is given by Equation 2 and for loads less that the results of Equation 4, the duty cycle is given Equation 3. For Equations 1 through 4, the variable definitions are as follows.

- V_{OUT} is the output voltage of the converter in V
- V_D is the forward conduction voltage drop across the rectifier or catch diode in V
- V_{IN} is the input voltage to the converter in V
- I_{OUT} is the output current of the converter in A
- L is the inductor value in H
- f_{SW} is the switching frequency in Hz

Setting the Oscillator Frequency

The oscillator frequency is determined by a resistor and capacitor connected to the RC pin of the TPS40210. The capacitor is charged to a level of approximately $V_{VDD}/20$ by current flowing through the resistor and is then discharged by a transistor internal to the TPS40210. The required resistor for a given oscillator frequency is found from either Figure 1 or Equation 5.

$$R_T = \frac{1}{5.8\times10^{-8}\times f_{SW}\times C_T + 8\times10^{-10}\times f_{SW}^{\,2} + 1.4\times10^{-7}\times f_{SW} - 1.5\times10^{-4} + 1.7\times10^{-6}\times C_T - 4\times10^{-9}\times C_T^{\,2}} \quad (5)$$

where

- R_T is the timing resistance in kΩ
- f_{SW} is the switching frequency in kHz
- C_T is the timing capacitance in pF

For most applications a capacitor in the range of 68 pF to 120 pF gives the best results. Resistor values should be limited to between 100 kΩ and 1 MΩ as well. If the resistor value falls below 100 kΩ, decrease the capacitor size and recalculate the resistor value for the desired frequency. As the capacitor size decreases below 47 pF, the accuracy of Equation 5 degrades and empirical means may be needed to fine tune the timing component values to achieve the desired switching frequency.

Synchronizing the Oscillator

The TPS40210 and TPS40211 can be synchronized to an external clock source. Figure 20 shows the functional diagram of the oscillator. When synchronizing the oscillator to an external clock, the RC pin must be pulled below 150 mV for 20 ns or more. The external clock frequency must be higher than the free running frequency of the converter as well. When synchronizing the controller, if the RC pin is held low for an excessive amount of time, erratic operation may occur. The maximum amount of time that the RC pin should be held low is 50% of a nominal output pulse, or 10% of the period of the synchronization frequency.

Under circumstances where the duty cycle is less than 50%, a Schottky diode connected from the RC pin to an external clock may be used to synchronize the oscillator. The cathode of the diode is connected to the RC pin. The trip point of the oscillator is set by an internal voltage divider to be 1/20 of the input voltage. The clock signal must have an amplitude higher than this trip point. When the clock goes low, it allows the reset current to restart the RC ramp, synchronizing the oscillator to the external clock. This provides a simple, single-component method for clock synchronization.

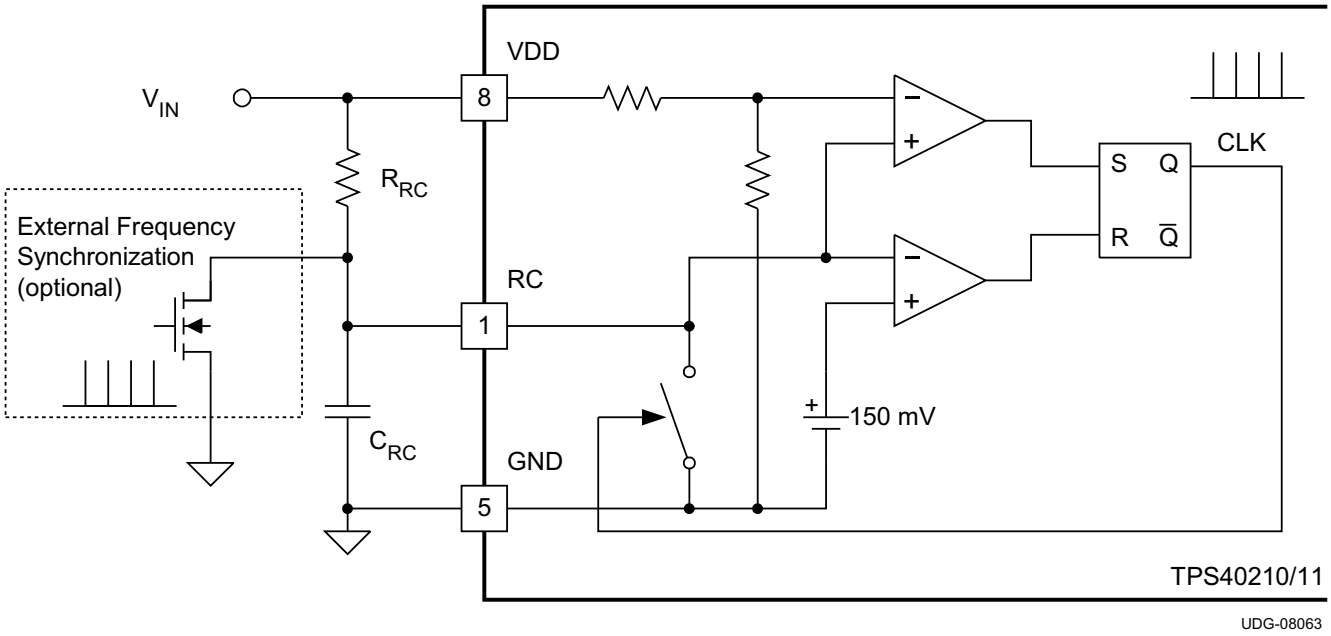


Figure 20. Oscillator Functional Diagram

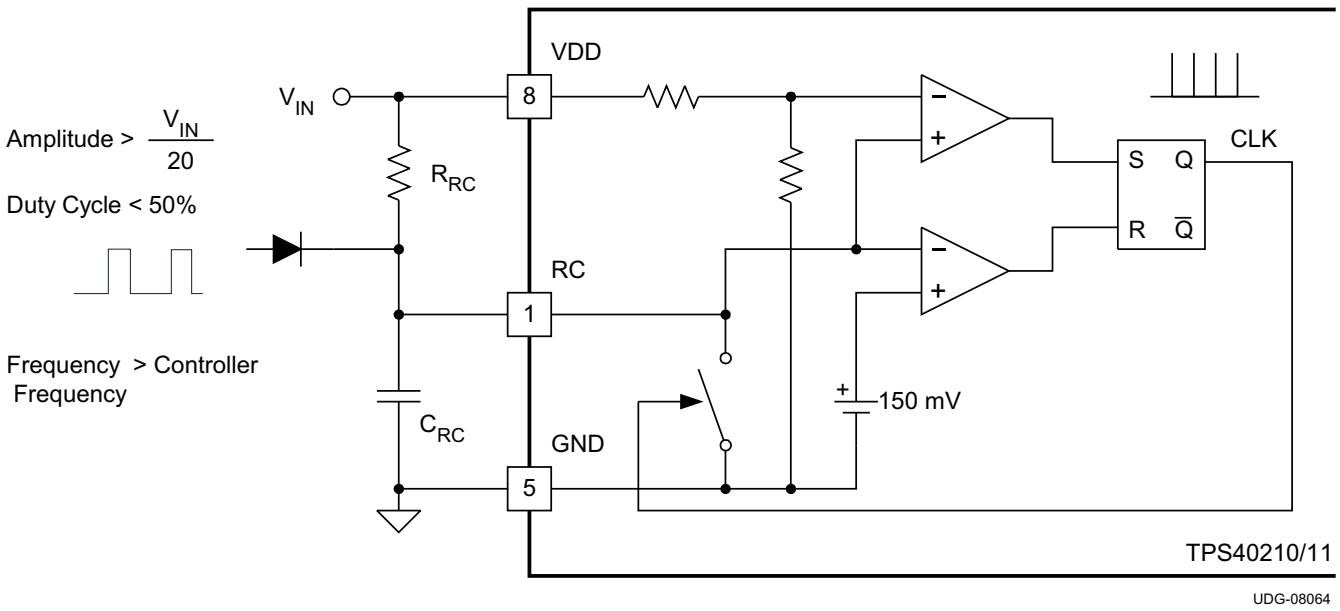


Figure 21. Diode Connected Synchronization

Current Sense and Overcurrent

The tps40210 and TPS40211 are current mode controllers and use a resistor in series with the source terminal power FET to sense current for both the current mode control and overcurrent protection. The device enters a current limit state if the voltage on the ISNS pin exceeds the current limit threshold voltage $V_{ISNS(oc)}$ from the electrical specifications table. When this happens the controller discharges the SS capacitor through a relatively high impedance and then attempt to restart. The amount of output current that causes this to happen is dependent on several variables in the converter.

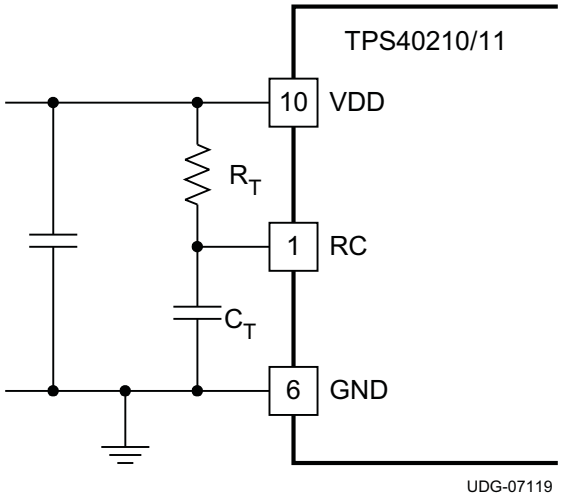


Figure 22. Oscillator Components

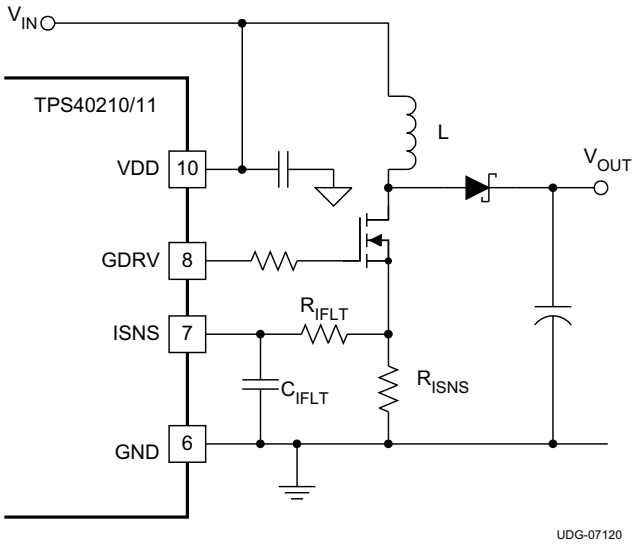


Figure 23. Current Sense Components

The load current overcurrent threshold is set by proper choice of R_{ISNS}. If the converter is operating in discontinuous mode the current sense resistor is found in Equation 6.

$$R_{ISNS} = \frac{f_{SW} \times L \times V_{ISNS(oc)}}{\sqrt{2 \times L \times f_{SW} \times I_{OUT(oc)} \times (V_{OUT} + V_D - V_{IN})}} \quad (6)$$

If the converter is operating in continuous conduction mode R_{ISNS} can be found in Equation 7.

$$R_{ISNS} = \frac{V_{ISNS}}{\left(\frac{I_{OUT}}{1-D}\right) + \left(\frac{I_{RIPPLE}}{2}\right)} = \frac{V_{ISNS}}{\left(\frac{I_{OUT}}{(1-D)}\right) + \left(\frac{D \times V_{IN}}{2 \times f_{SW} \times L}\right)} \quad (7)$$

where

- R_{ISNS} is the value of the current sense resistor in Ω.
- $V_{ISNS(oc)}$ is the overcurrent threshold voltage at the ISNS pin (from electrical specifications)
- D is the duty cycle (from Equation 2)
- f_{SW} is the switching frequency in Hz
- V_{IN} is the input voltage to the power stage in V (see text)
- L is the value of the inductor in H
- I_{OUT}(oc) is the desired overcurrent trip point in A
- V_D is the drop across the diode in Figure 23

The TPS40210/11 has a fixed undervoltage lockout (UVLO) that allows the controller to start at a typical input voltage of 4.25 V. If the input voltage is slowly rising, the converter might have less than its designed nominal input voltage available when it has reached regulation. As a result, this may decreases the apparent current limit load current value and must be taken into consideration when selecting R_{ISNS}. The value of V_{IN} used to calculate R_{ISNS} must be the value at which the converter finishes startup. The total converter output current at startup is the sum of the external load current and the current required to charge the output capacitor(s). See the *Soft Start* section of this datasheet for information on calculating the required output capacitor charging current.

The topology of the standard boost converter has no method to limit current from the input to the output in the event of a short circuit fault on the output of the converter. If protection from this type of event is desired, it is necessary to use some secondary protection scheme such a fuse or rely on the current limit of the upstream power source.

Current Sense and Sub-Harmonic Instability

A characteristic of peak current mode control results in a condition where the current control loop can exhibit instability. This results in alternating long and short pulses from the pulse width modulator. The voltage loop maintains regulation and dioes not oscillate, but the output ripple voltage increases. The condition occurs only when the converter is operating in continuous conduction mode and the duty cycle is 50% or greater. The cause of this condition is described in Texas Instruments literature number SLUA101, available at www.ti.com. The remedy for this condition is to apply a compensating ramp from the oscillator to the signal going to the pulse width modulator. In the TPS40210/11 the oscillator ramp is applied in a fixed amount to the pulse width modulator. The slope of the ramp is given in Equation 8.

$$s_e = f_{SW} \times \left(\frac{V_{VDD}}{20}\right) \quad (8)$$

To ensure that the converter does not enter into sub-harmonic instability, the slope of the compensating ramp signal must be at least half of the down slope of the current ramp signal. Since the compensating ramp is fixed in the TPS40210/11, this places a constraint on the selection of the current sense resistor.

The down slope of the current sense wave form at the pulse width modulator is described in Equation 9.

$$m2 = \frac{A_{CS} \times R_{ISNS} \times (V_{OUT} + V_D - V_{IN})}{L} \quad (9)$$

Since the slope compensation ramp must be at least half, and preferably equal to the down slope of the current sense waveform seen at the pulse width modulator, a maximum value is placed on the current sense resistor

when operating in continuous mode at 50% duty cycle or greater. For design purposes, some margin should be applied to the actual value of the current sense resistor. As a starting point, the actual resistor chosen should be 80% or less that the value calculated in Equation 10. This equation calculates the resistor value that makes the slope compensation ramp equal to one half of the current ramp downslope. Values no more than 80% of this result would be acceptable.

$$R_{ISNS(max)} = \frac{V_{VDD} \times L \times f_{SW}}{60 \times (V_{OUT} + V_D - V_{IN})} \quad (10)$$

where

- S_e is the slope of the voltage compensating ramp applied to the pulse width modulator in V/s
- f_{SW} is the switching frequency in Hz
- V_{VDD} is the voltage at the VDD pin in V
- m2 is the down slope of the current sense waveform seen at the pulse width modulator in V/s
- R_{ISNS} is the value of the current sense resistor in Ω
- V_{OUT} is the converter output voltage V_{IN} is the converter power stage input voltage
- V_D is the drop across the diode in Figure 23

It is possible to increase the voltage compensation ramp slope by connecting the VDD pin to the output voltage of the converter instead of the input voltage as shown in Figure 23. This can help in situations where the converter design calls for a large ripple current value in relation to the desired output current limit setting.

NOTE:

Connecting the VDD pin to the output voltage of the converter affects the startup voltage of the converter since the controller undervoltage lockout (UVLO) circuit monitors the VDD pin and senses the input voltage less the diode drop before startup. The effect is to increase the startup voltage by the value of the diode voltage drop.

If an acceptable R_{ISNS} value is not available, the next higher value can be used and the signal from the resistor divided down to an acceptable level by placing another resistor in parallel with C_{ISNS}.

Current Sense Filtering

In most cases, a small filter placed on the ISNS pin improves performance of the converter. These are the components R_{IFLT} and C_{IFLT} in Figure 23. The time constant of this filter should be approximately 10% of the nominal pulse width of the converter. The pulse width can be found using Equation 11.

$$t_{ON} = \frac{D}{f_{SW}} \quad (11)$$

The suggested time constant is then

$$R_{IFLT} \times C_{IFLT} = 0.1 \times t_{ON} \quad (12)$$

The range of R_{IFLT} should be from about 1 kΩ to 5 kΩ for best results. Higher values can be used but this raises the impedance of the ISNS pin connection more than necessary and can lead to noise pickup issues in some layouts. C_{ISNS} should be located as close as possible to the ISNS pin as well to provide noise immunity.

Soft Start

The soft-start feature of the TPS40210/11 is a closed loop soft start, meaning that the output voltage follows a linear ramp that is proportional to the ramp generated at the SS pin. This ramp is generated by an internal resistor connected from the BP pin to the SS pin and an external capacitor connected from the SS pin to GND. The SS pin voltage (V_{SS}) is level shifted down by approximately $V_{SS(ofst)}$ (approximately 700 mV) and sent to one of the “+” (the “+” input with the lowest voltage dominates) inputs of the error amplifier. When this level shifted voltage (V_{SSE}) starts to rise at time t_1 (see Figure 24), the output voltage the controller expects, rises as well. Since V_{SSE} starts at near 0 V, the controller attempts to regulate the output voltage from a starting point of zero volts. It cannot do this due to the converter architecture. The output voltage starts from the input voltage less the

drop across the diode (V_{IN} - V_D) and rise from there. The point at which the output voltage starts to rise (t_2) is the point where the V_{SSE} ramp passes the point where it is commanding more output voltage than (V_{IN} - V_D). This voltage level is labeled $V_{SSE(1)}$. The time required for the output voltage to ramp from a theoretical zero to the final regulated value (from t_1 to t_3) is determined by the time it takes for the capacitor connected to the SS pin (C_{SS}) to rise through a 700 mV range, beginning at $V_{SS(ofst)}$ above GND.

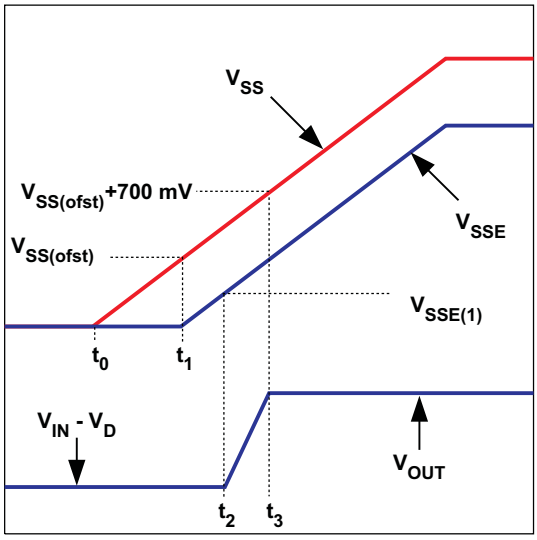


Figure 24. SS Pin Voltage adn Output Voltage

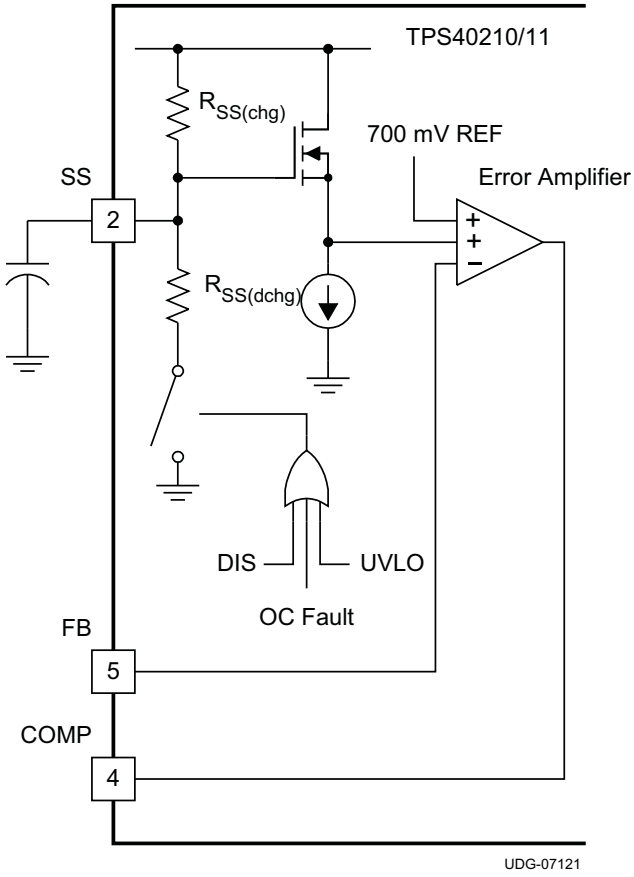


Figure 25. SS Pin Functional Circuit

The required capacitance for a given soft start time $t_3 - t_1$ in Figure 24 is calculated in Equation 13.

$$C_{SS} = \frac{t_{SS}}{R_{SS} \times \ln\left(\frac{V_{BP} - V_{SS(ofst)}}{V_{BP} - \left(V_{SS(ofst)} + V_{FB}\right)}\right)} \quad (13)$$

where

- t_{SS} is the soft-start time
- $R_{SS(chg)}$ is the SS charging resistance in Ω, typically 500 kΩ
- C_{SS} is the value of the capacitor on the SS pin, in F
- V_{BP} is the value of the voltage on the BP pin in V
- $V_{SS(ofst)}$ is the approximate level shift from the SS pin to the error amplifier (~700 mV)
- V_{FB} is the error amplifier reference voltage, 700m V typical

Note that t_{SS} is the time it takes for the output voltage to rise from 0 V to the final output voltage. Also note the tolerance on $R_{SS(chg)}$ given in the electrical specifications table. This contributes to some variability in the output voltage rise time and margin must be applied to account for it in design.

Also take note of V_{BP}. Its value varies depending on input conditions. For example, a converter operating from a slowly rising input initializes V_{BP} at a fairly low value and increases during the entire startup sequence. If the controller has a voltage above 8 V at the input and the DIS pin is used to stop and then restart the converter, V_{BP} is approximately 8 V for the entire startup sequence. The higher the voltage on BP, the shorter the startup time is and conversely, the lower the voltage on BP, the longer the startup time is.

The soft-start time (t_{SS}) must be chosen long enough so that the converter can start up without going into an overcurrent state. Since the over current state is triggered by sensing the peak voltage on the ISNS pin, that voltage must be kept below the overcurrent threshold voltage $V_{ISNS(oc)}$. The voltage on the ISNS pin is a function of the load current of the converter, the rate of rise of the output voltage and the output capacitance, and the current sensing resistor. The total output current that must be supported by the converter is the sum of the charging current required by the output capacitor and any external load that must be supplied during startup. This current must be less than the $I_{OUT(oc)}$ value used in Equation 6 or Equation 7 (depending on the operating mode of the converter) to determine the current sense resistor value. In these equations, the actual input voltage at the time that the controller reaches the final output voltage is the important input voltage to use in the calculations. If the input voltage is slowly rising and is at less than the nominal input voltage when the startup time ends, the output current limit is less than $I_{OUT(oc)}$ at the nominal input voltage. The output capacitor charging current must be reduced (decrease C_{OUT} or increase the t_{SS}) or $I_{OUT(oc)}$ must be increased and a new value for R_{ISNS} calculated.

$$I_{C(chg)} = \left(\frac{C_{OUT} \times V_{OUT}}{t_{SS}} \right) \tag{14}$$

$$t_{SS} > \left(\frac{C_{OUT} \times V_{OUT}}{(I_{OUT(oc)} - I_{EXT})} \right) \tag{15}$$

where

- $I_{C(chg)}$ is the output capacitor charging current in A
- C_{OUT} is the total output capacitance in F
- V_{OUT} is the output voltage in V
- t_{SS} is the soft start time from Equation 13
- $I_{OUT(oc)}$ is the desired over current trip point in A
- I_{EXT} is any external load current in A

The capacitor on the SS pin (C_{SS}) also plays a role in overcurrent functionality. It is used as the timer between restart attempts. The SS pin is connected to GND through a resistor, $R_{SS(dchg)}$, whenever the controller senses an overcurrent condition. Switching stops and nothing else happens until the SS pin discharges to the soft-start reset threshold, $V_{SS(rst)}$. At this point, the SS pin capacitor is allowed to charge again through the charging resistor $R_{SS(chg)}$, and the controller restarts from that point. The shortest time between restart attempts occurs when the SS pin discharges from $V_{SS(ofst)}$ (approximately 700 mV) to $V_{SS(rst)}$ (150 mV) and then back to $V_{SS(ofst)}$ and switching resumes. In actuality, this is a conservative estimate since switching does not resume until the V_{SSE} ramp rises to a point where it is commanding more output voltage than exists at the output of the controller. This occurs at some SS pin voltage greater than $V_{SS(ofst)}$ and depends on the voltage that remains on the output overvoltage the converter while switching has been halted. The fastest restart time can be calculated by using Equation 16, Equation 17 and Equation 18.

$$t_{DCHG} = R_{SS(dchg)} \times C_{SS} \times \ln\left(\frac{V_{SS(ofst)}}{V_{SS(rst)}}\right) \quad (16)$$

$$t_{CHG} = R_{SS(chg)} \times C_{SS} \times \ln\left(\frac{\left(V_{BP} - V_{SS(rst)}\right)}{\left(V_{BP} - V_{SS(ofst)}\right)}\right) \quad (17)$$

$$t_{RSTRT(min)} = t_{CHG} + t_{DCHG} \quad (18)$$

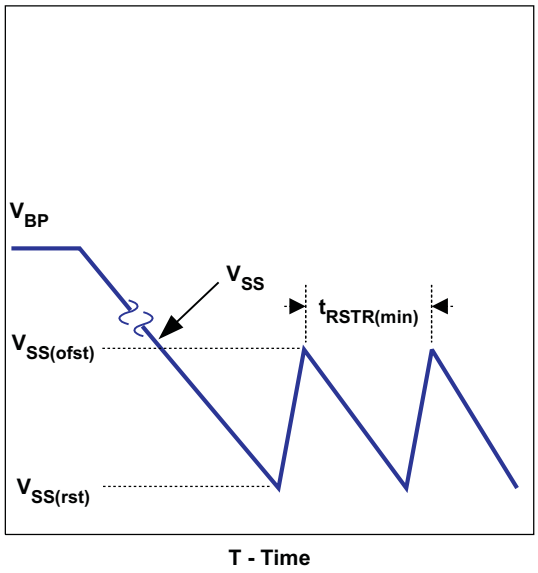


Figure 26. Soft Start During Overcurrent

BP Regulator

The TPS40210/11 has an on board linear regulator the supplies power for the internal circuitry of the controller, including the gate driver. This regulator has a nominal output voltage of 8 V and must be bypassed with a 1-µF capacitor. If the voltage at the VDD pin is less than 8 V, the voltage on the BP pin ia also be less and the gate drive voltage to the external FET ia reduced from the nominal 8 V. This should be considered when choosing a FET for the converter.

Connecting external loads to this regulator can be done, but care must be taken to ensure that the thermal rating of the device is observed since is no thermal shutdown feature in this controller. Exceeding the thermal ratings cause out of specification behavior and can lead to reduced reliability. The controller dissipates more power when there is an external load on the BP pin and is tested for dropout voltage for up to 5-mA load. When the controller is in the disabled state, the BP pin regulator also shuts off so loads connected there power down as well. When the controller is disabled with the DIS/$\overline{EN}$ pin, this regulator is turned off.

The total power dissipation in the controller can be calculated as follows. The total power is the sum of P_Q, P_G and P_E.

$$P_Q = V_{VDD} \times I_{VDD(en)} \tag{19}$$

$$P_G = V_{VDD} \times Q_g \times f_{SW} \tag{20}$$

$$P_E = V_{VDD} \times I_{EXT} \tag{21}$$

where

- P_Q is the quiescent power of the device in W
- V_{VDD} is the VDD pin voltage in V
- $I_{VDD(en)}$ is the quiescent current of the controller when enabled but not switching in A
- P_G is the power dissipated by driving the gate of the FET in W
- Q_g is the total gate charge of the FET at the voltage on the BP pin in C
- f_{SW} is the switching frequency in Hz
- P_E is the dissipation caused be external loading of the BP pin in W
- I_{EXT} is the external load current in A

Shutdown (DIS/$\overline{EN}$ Pin)

The DIS/$\overline{EN}$ pin is an active high shutdown command for the controller. Pulling this pin above 1.2 V causes the controller to completely shut down and enter a low current consumption state. In this state, the regulator connected to the BP pin is turned off. There is an internal 1.1-MΩ pull-down resistor connected to this pin that keeps the pin at GND level when left floating. If this function is not used in an application, it is best to connect this pin to GND

Control Loop Considerations

There are two methods to design a suitable control loop for the TPS4021x. The first and preferred if equipment is available is to use a frequency response analyzer to measure the open loop modulator and power stage gain and to then design compensation to fit that. The usage of these tools for this purpose is well documented with the literature that accompanies the tool and is not be discussed here.

The second option is to make an initial guess at compensation, and then evaluate the transient response of the system to see if the compensation is acceptable to the application or not. For most systems, an adequate response can be obtained by simply placing a series resistor and capacitor (R_{FB} and C_{FB}) from the COMP pin to the FB pin as shown in Figure 27.

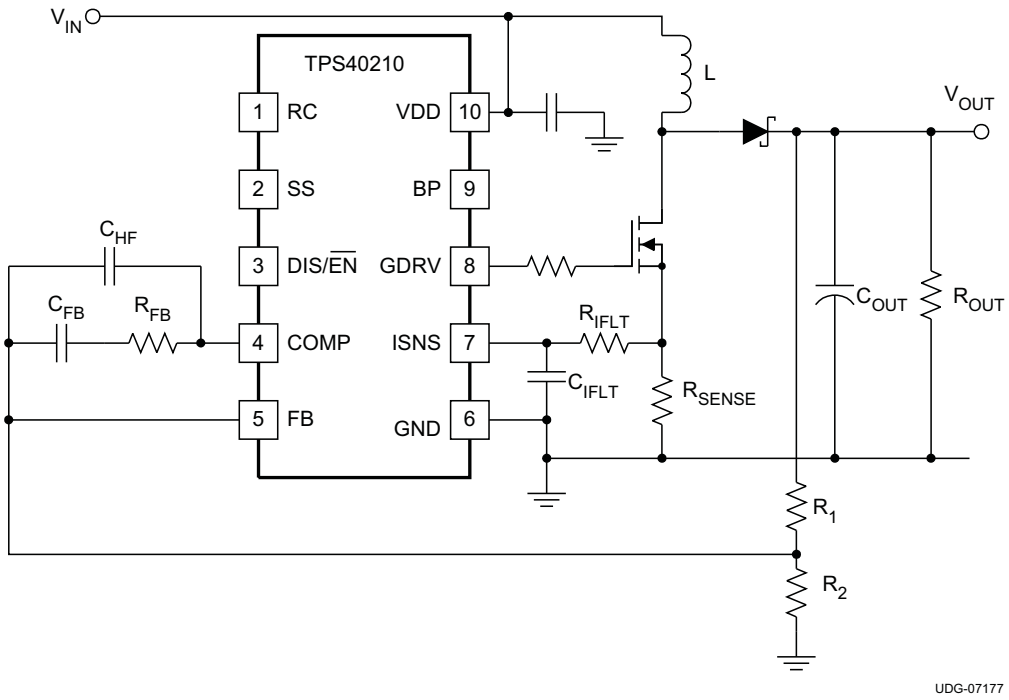


Figure 27. Basic Compensation Network

The natural phase characteristics of most capacitors used for boost outputs combined with the current mode control provide adequate phase margin when using this type of compensation. To determine an initial starting point for the compensation, the desired crossover frequency must be considered when estimating the control to output gain. The model used is a current source into the output capacitor and load.

When using these equations, the loop bandwidth should be no more than 20% of the switching frequency, f_{SW}. A more reasonable loop bandwidth would be 10% of the switching frequency. Be sure to evaluate the transient response of the converter over the expected load range to ensure acceptable operation.

$$\left|K_{CO}\right| = g_M \times \left|Z_{OUT}\left(f_{CO}\right)\right| = 19.1\,\frac{A}{V} \times 0.146\,\Omega = 2.80 \tag{22}$$

$$g_M = \frac{0.13 \times \sqrt{L \times \frac{f_{SW}}{R_{OUT}}}}{\left(R_{ISNS}\right)^2 \times \left(120 \times R_{ISNS} + L \times f_{SW}\right)} = \frac{0.13 \times \sqrt{10\,\mu H \times \frac{600\,kHz}{240\,\Omega}}}{\left(12\,m\Omega\right)^2 \times \left(120 \times 12\,m\Omega + 10\,\mu H \times 600\,kHz\right)} = 19.1\,\frac{A}{V} \tag{23}$$

$$\left|Z_{OUT}\right| = R_{OUT} \times \sqrt{\frac{\left(1 + \left(2\pi \times f_L \times R_{ESR} \times C_{OUT}\right)^2\right)}{1 + \left(\left(R_{OUT}\right)^2 + 2 \times R_{OUT} \times R_{ESR} + \left(R_{ESR}\right)^2\right) \times \left(2\pi \times f_L \times C_{OUT}\right)^2}} \tag{24}$$

where

- K_{CO} is the control to output gain of the converter, in V/V
- g_M is the transconductance of the power stage and modulator, in S
- R_{OUT} is the output load equivalent resistance, in Ω
- Z_{OUT} is the output impedance, including the output capacitor, in Ω
- R_{ISNS} is the value of the current sense resistor, in Ω
- L is the value of the inductor, in H
- C_{OUT} is the value of the output capacitance, in µF
- R_{ESR} is the equivalent series resistance of C_{OUT}, in Ω
- f_{SW} is the switching frequency, in Hz
- f_L is the desired crossover frequency for the control loop, in Hz

These equations assume that the operation is discontinuous and that the load is purely resistive. The gain in continuous conduction can be found by evaluating Equation 23 at the resistance that gives the critical conduction current for the converter. Loads that are more like current sources give slightly higher gains than predicted here. To find the gain of the compensation network required for a control loop of bandwidth f_L, take the reciprocal of Equation 22.

$$K_{COMP} = \frac{1}{\left|K_{CO}\right|} = \frac{1}{2.80} = 0.356 \tag{25}$$

The GBWP of the error amplifier is only guaranteed to be at least 1.5 MHz. If K_{COMP} multiplied by the f_L is greater than 750 kHz, reduce the desired loop crossover frequency until this condition is satisfied. This ensures that the high-frequency pole from the error amplifier response with the compensation network in place does not cause excessive phase lag at the f_L and decrease phase margin in the loop.

The R-C network connected from COMP to FB places a zero in the compensation response. That zero should be approximately 1/10th of the desired crossover frequency, f_L. With that being the case, R_{FB} and C_{FB} can be found from Equation 26 and Equation 27

$$R_{FB} = \frac{R1}{\left|K_{CO}\right|} = R1 \times K_{COMP} \tag{26}$$

$$C_{FB} = \frac{10}{2\pi \times f_L \times R_{FB}} \tag{27}$$

where

- R1 is in f_L is the loop crossover frequency desired, in Hz
- R_{FB} is the feedback resistor in C_{FB} is the feedback capacitance in µF.

Thought not strictly necessary, it is recommended that a capacitor be added between COMP and FB to provide high-frequency noise attenuation in the control loop circuit. This capacitor introduces another pole in the compensation response. The allowable location of that pole frequency determines the capacitor value. As a starting point, the pole frequency should be 10 × f_L. The value of C_{HF} can be found from Equation 28.

$$C_{HF} = \frac{1}{20\pi \times f_L \times R_{FB}} \quad (28)$$

The error amplifier GBWP will usually be higher, but is ensured by design to be at least 1.5 MHz. If the gain required in Equation 25 multiplied by 10 times the desired control loop crossover frequency, the high-frequency pole introduced by C_{HF} is overridden by the error amplifier capability and the effective pole is lower in frequency. If this is the case, C_{HF} can be made larger to provide a consistent high-frequency roll off in the control loop design. Equation 29 calculates the required C_{HF} in this case.

$$C_{HF} = \frac{1}{2\pi \times 1.5 \times (10)^6 \times R_{FB}} \quad (29)$$

where

- C_{HF} is the high-frequency roll-off capacitor value in µF
- R_{FB} is the mid band gain setting resistor value in Ω

GATE DRIVE CIRCUIT

Some applications benefit from the addition of a resistor connected between the GDRV pin and the gate of the switching MOSFET. In applications that have particularly stringent load regulation (under 0.75%) requirements and operate from input voltages above 5 V, or are sensitive to pulse jitter in the discontinuous conduction region, this resistor is recommended. The recommended starting point for the value of this resistor can be calculated from Equation 30.

$$R_G = \frac{105}{Q_G} \quad (30)$$

where

- Q_G is the MOSFET total gate charge at 8-V V_{GS} in nC
- R_G is the suggested starting point gate resistance in Ω

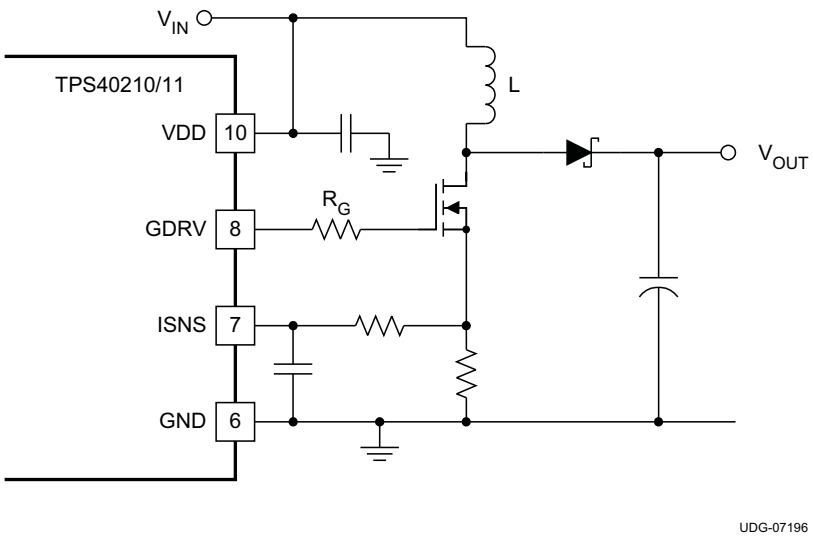


Figure 28. Gate Drive Resistor

TPS40211

The only difference between the TPS40210 and the TPS40211 is the reference voltage that the error amplifier uses to regulate the output voltage. The TPS40211 uses a 260-mV reference and is intended for applications where the output is actually a current instead of a regulated voltage. A typical example of an application of this type is an LED driver. An example schematic is shown in Figure 29.

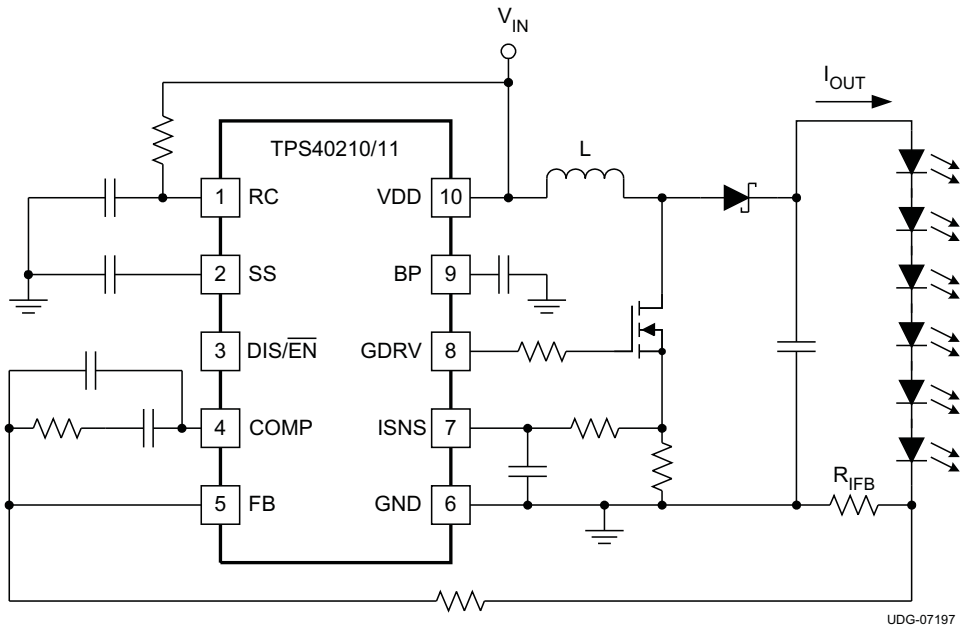


Figure 29. Typical LED Drive Schematic

The current in the LED string is set by the choice of the resistor R_{ISNS} as shown in Equation 31.

$$R_{IFB} = \frac{V_{FB}}{I_{OUT}} \tag{31}$$

where

- R_{IFB} is the value of the current sense resistor for the LED string in Ω
- V_{FB} is the reference voltage for the TPS40211 in V (0.260 V typ)
- I_{OUT} is the desired DC current in the LED string in A

ADDITIONAL REFERENCES

Related Devices

The following devices have characteristics similar to the TPS40210 and may be of interest.

Related Parts

DEVICE	DESCRIPTION
TPS6100X	Single- and Dual-Cell Boost Converter with Strart-up into Full Load
TPS6101X	High Efficiency 1-Cell and 2-Cell Bost Converters
TPS6300X	High Effiency Single Inductor Buck-Boost Converter with 1.8A Switches

References

These references may be found on the web at www.power.ti.com under Technical Documents. Many design tools and links to additional references, may also be found at www.power.ti.com

1. *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SEM 1400, 2001 Seminar Series
2. *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series
3. Additional PowerPAD™ information may be found in Applications Briefs SLMA002 and SLMA004
4. QFN/SON PCB Attachment, Texas Instruments Literature Number SLUA271, June 2002

DESIGN EXAMPLE 1

12-V to 24-V Non-Synchronous Boost Regulator

The following example illustrates the design process and component selection for a 12-V to 24-V non-synchronous boost regulator using the TPS40210 controller.

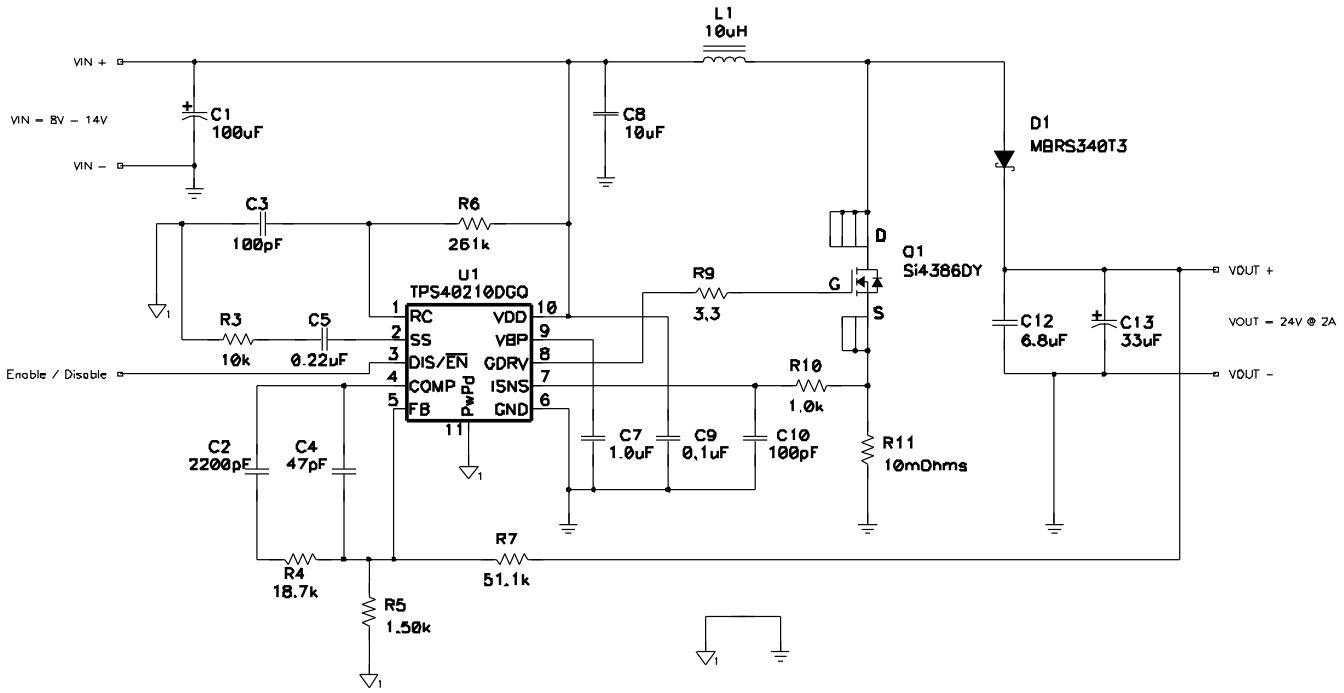


Figure 30. TPS40210 Design Example – 8-V to 24-V at 2-A

TPS40210 Design Example Specifications

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current			4.4		A
	No load input current				0.05	
$V_{IN(UVLO)}$	Input undervoltage lockout			4.5		V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage		23.5	24.0	24.5	V
	Line regulation				1%	
	Load regulation				1%	
$V_{OUT(ripple)}$	Output voltage ripple				500	mV_{PP}
I_{OUT}	Output current	8 V ≤ V_{IN} ≤ 14 V	0.2	1	2.0	A
I_{OCP}	Output overcurrent inception point		3.5			
	Transient response					
ΔI	Load step			1		A
	Load slew rate			1		A/µs
	Overshoot threshold voltage			500		mV
	Settling time			5		ms

TPS40210 Design Example Specifications (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency			600		kHz
η_{PK}	Peak efficiency	V_{IN} = 12 V, 0.2 A ≤ I_{OUT} ≤ 2 A		95%		
η	Full load efficiency	V_{IN} = 12 V, I_{OUT} = 2 A		94%		
T_{OP}	Operating temperature range	10 V ≤ V_{IN} ≤ 14 V, 0.2 A ≤ I_{OUT} ≤ 2 A		25		°C
MECHANICAL DIMENSIONS						
W	Width			1.5		in
L	Length			1.5		
h	Height			0.5		

Step-By-Step Design Procedure

Duty Cycle Estimation

The duty cycle of the main switching MOSFET is estimated using Equation 32 and Equation 33.

$$D_{MIN} \approx \frac{V_{OUT} - V_{IN(max)} + V_{FD}}{V_{OUT} + V_{FD}} = \frac{24\,V - 14\,V + 0.5\,V}{24\,V + 0.5\,V} = 42.8\% \quad (32)$$

$$D_{MAX} \approx \frac{V_{OUT} - V_{IN(min)} + V_{FD}}{V_{OUT} + V_{FD}} = \frac{24\,V - 8\,V + 0.5\,V}{24\,V + 0.5\,V} = 67.3\% \quad (33)$$

Using and estimated forward drop of 0.5 V for a schottkey rectifier diode, the approximate duty cycle is 42.8% (minimum) to 67.3% (maximum).

Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current.

$$I_{Lrip(max)} = 0.3 \times \frac{I_{OUT(max)}}{1 - D_{MIN}} = 0.3 \times \frac{2}{1 - 0.428} = 1.05\,A \quad (34)$$

The minimum inductor size can be estimated using Equation 35.

$$L_{MIN} \approx \frac{V_{IN(max)}}{I_{Lrip(max)}} \times D_{MIN} \times \frac{1}{f_{SW}} = \frac{14\,V}{1.05\,A} \times 0.673 \times \frac{1}{600\,kHz} = 9.5\,\mu H \quad (35)$$

The next higher standard inductor value of 10 µH is selected. The ripple current is estimated by Equation 36.

$$I_{RIPPLE} \approx \frac{V_{IN}}{L} \times D \times \frac{1}{f_{SW}} = \frac{12\,V}{10\,\mu H} \times 0.50 \times \frac{1}{600\,kHz} = 1.02\,A \quad (36)$$

$$I_{RIPPLE(Vinmin)} \approx \frac{V_{IN}}{L} \times D \times \frac{1}{f_{SW}} = \frac{8\,V}{10\,\mu H} \times 0.673 \times \frac{1}{600\,kHz} = 0.89\,A \quad (37)$$

The worst case peak-to-peak ripple current occurs at 50% duty cycle and is estimated as 1.02 A. Worst case RMS current through the inductor is approximated by Equation 38.

$$I_{Lrms} = \sqrt{\left(I_{L(avg)}\right)^2 + \left(\tfrac{1}{12} I_{RIPPLE}\right)^2} \approx \sqrt{\left(\frac{I_{OUT(max)}}{1 - D_{MAX}}\right)^2 + \left(\tfrac{1}{12} I_{RIPPLE(VINmin)}\right)^2} = \sqrt{\left(\frac{2}{1 - 0.673}\right)^2 + \left(\left(\tfrac{1}{12}\right) \times 0.817\,A\right)^2} = 6.13\,Arms \quad (38)$$

The worst case RMS inductor current is 6.13 Arms. The peak inductor current is estimated by Equation 39.

$$I_{Lpeak} \approx \frac{I_{OUT(max)}}{1-D_{MAX}} + \left(\frac{1}{2}\right) I_{RIPPLE(Vinmin)} = \frac{2}{1-0.673} + \left(\frac{1}{2}\right) 0.718 = 6.57\,A \quad (39)$$

A 10-µH inductor with a minimum RMS current rating of 6.13 A and minimum saturation current rating of 6.57 A must be selected. A TDK RLF12560T-100M-7R5 7.5-A 10-µH inductor is selected.

This inductor power dissipation is estimated by Equation 40.

$$P_L \approx (I_{Lrms})^2 \times DCR \quad (40)$$

The TDK RLF12560T-100M-7R5 12.4-mΩ DCR dissipates 466 mW of power.

Rectifier Diode Selection

A low-forward voltage drop schottky diode is used as a rectifier diode to reduce its power dissipation and improve efficiency. Using 80% derating, on V_{OUT} for ringing on the switch node, the rectifier diode minimum reverse break-down voltage is given by Equation 41.

$$V_{(BR)R(min)} \geq \frac{V_{OUT}}{0.8} = 1.25 \times V_{OUT} = 1.25 \times 24\,V = 30\,V \quad (41)$$

The diode must have reverse breakdown voltage greater than 30 V. The rectifier diode peak and average currents are estimated by Equation 42 and Equation 43.

$$I_{D(avg)} \approx I_{OUT(max)} = 2\,A \quad (42)$$

$$I_{D(peak)} = I_{L(peak)} = 6.57\,A \quad (43)$$

For this design, 2-A average and 6.57-A peak is

The power dissipation in the diode is estimated by Equation 44.

$$P_{D(max)} \approx V_F \times I_{OUT(max)} = 0.5\,V \times 2\,A = 1W \quad (44)$$

For this design, the maximum power dissipation is estimated as 1 W. Reviewing 30-V and 40-V schottky diodes, the MBRS340T3, 40-V, 3-A diode in an SMC package is selected. This diode has a forward voltage drop of 0.48-V at 6-A, so the conduction power dissipation is approximately 960 mW, less than half its rated power dissipation.

Output Capacitor Selection

Output capacitors must be selected to meet the required output ripple and transient specifications.

$$C_{OUT} = 8\frac{I_{OUT} \times D}{V_{OUT(ripple)}} \times \frac{1}{f_{SW}} = 8\left(\frac{2\,A \times 0.673}{500\,mV}\right) \times \frac{1}{600\,kHz} = 35\,\mu F \quad (45)$$

$$ESR = \frac{7}{8} \times \frac{V_{OUT(ripple)}}{I_{L(peak)} - I_{OUT}} = \frac{7}{8} \times \frac{500\,mV}{6.57\,A - 2\,A} = 95\,m\Omega \quad (46)$$

A Panasonic EEEFC1V330P 35V 33-µF, 120-mΩ bulk capacitor and 6.8-µF ceramic capacitor is selected to provide the required capacitance and ESR at the switching frequency. The combined capacitance of 39.8 µF and 60 mΩ are used in compensation calculations.

Input Capacitor Selection

Since a boost converter has continuous input current, the input capacitor senses only the inductor ripple current. The input capacitor value can be calculated by Equation 47 and Equation 48 .

$$C_{IN} > \frac{I_{L(ripple)}}{4 \times V_{IN(ripple)} \times f_{SW}} = \frac{1.02\,A}{4 \times 60\,mV \times 600\,kHz} = 7.0\,\mu F \quad (47)$$

$$ESR < \frac{V_{IN(ripple)}}{2 \times I_{L(ripple)}} = \frac{60\,mV}{2 \times 1.02\,A} = 30\,m\Omega \quad (48)$$

For this design, to meet a maximum input ripple of 60 mV, a minimum 7.0-µF input capacitor with ESR less than 30 mΩ is needed. A 10-µF X7R ceramic capacitor is selected.

Current Sense and Current Limit

The maximum allowable current sense resistor value is limited by both the current limit and sub-harmonic stability. These two limitations are given by Equation 49 and Equation 50.

$$R_{ISNS} < \frac{V_{OCP(min)}}{1.1 \times \left(I_{L(peak)} + I_{Drive}\right)} = \frac{110\,mV}{1.1 \times 6.57\,A + 0.50\,A} = 14.2\,m\Omega \quad (49)$$

$$R_{ISNS} < \frac{VDD_{MAX} \times L \times f_{SW}}{60 \times (V_{OUT} + V_{fd} - V_{IN})} = \frac{14\,V \times 10\,\mu H \times 600\,kHz}{60 \times (24\,V + 0.48\,V - 14\,V)} = 133\,m\Omega \quad (50)$$

The current limit requires a resistor less than 14.2 mΩ and stability requires a sense resistor less than 133 mΩ. A 10-mΩ resistor is selected. Approximately 2-mΩ of routing resistance added in compensation calculations.

Current Sense Filter

To remove switching noise from the current sense, an R-C filter is placed between the current sense resistor and the ISNS pin. A resistor with a value between 1 kΩ and 5 kΩ is selected and a capacitor value is calculated by Equation 51.

$$C_{IFLT} = \frac{0.1 \times D_{MIN}}{f_{SW} \times R_{IFLT}} = \frac{0.1 \times 0.428}{600\,kHz \times 1k\Omega} = 71pF \quad (51)$$

For a 1-kΩ filter resistor, 71 pF is calculated and a 100-pF capacitor is selected.

Switching MOSFET Selection

The TPS40210 drives a ground referenced N-channel FET. The $R_{DS(on)}$ and gate charge are estimated based on the desired efficiency target.

$$P_{DISS(total)} \approx P_{OUT} \times \left(\frac{1}{\eta} - 1\right) = V_{OUT} \times I_{OUT} \times \left(\frac{1}{\eta} - 1\right) = 24\,V \times 2\,A \times \left(\frac{1}{0.95} - 1\right) = 2.526\,W \quad (52)$$

For a target of 95% efficiency with a 24 V Input voltage at 2 A, maximum power dissipation is limited to 2.526 W. The main power dissipating devices are the MOSFET, inductor, diode, current sense resistor and the integrated circuit, the TPS40210.

$$P_{FET} < P_{DISS(total)} - P_L - P_D - P_{Risns} - V_{IN(max)} \times I_{VDD} \quad (53)$$

This leaves 740 mW of power dissipation for the MOSFET. This can likely cause an SO-8 MOSFET to get too hot, so power dissipation is limited to 500 mW. Allowing half for conduction and half for switching losses, we can determine a target $R_{DS(on)}$ and Q_{GS} for the MOSFET by Equation 54 and Equation 55.

$$Q_{GS} < \frac{3 \times P_{FET} \times I_{DRIVE}}{2 \times V_{OUT} \times I_{OUT} \times f_{SW}} = \frac{3 \times 0.50\,W \times 0.50\,A}{2 \times 24\,V \times 2\,A \times 600\,kHz} = 13.0\,nC \quad (54)$$

A target MOSFET gate-to-source charge of less than 13.0 nC is calculated to limit the switching losses to less than 250 mW.

$$R_{DS(on)} < \frac{P_{FET}}{2 \times (I_{RMS})^2 \times D} = \frac{0.50\,W}{2 \times 6.13^2 \times 0.674} = 9.8\,m\Omega \quad (55)$$

A target MOSFET $R_{DS(on)}$ of 9.8 mΩ is calculated to limit the conduction losses to less than 250 mW. Reviewing 30-V and 40-V MOSFETs, an Si4386DY 9-mΩ MOSFET is selected. A gate resistor was added per equation (30). The maximum gate charge at Vgs=8 V for the Si4386DY is 33.2 nC, this impiles RG = 3.3 Ω.

Feedback Divider Resistors

The primary feedback divider resistor (R_{FB}) from VOUT to FB should be selected between 10-kΩ and 100-kΩ to maintain a balance between power dissipation and noise sensitivity. For a 24-V output a high feedback resistance is desirable to limit power dissipation so R_{FB} = 51.1 kΩ is selected.

$$R_{BIAS} = \frac{V_{FB} \times R_{FB}}{V_{OUT} - V_{FB}} = \frac{0.700\,V \times 51.1k\Omega}{24\,V - 0.700\,V} = 1.53k\Omega \quad (56)$$

R_{BIAS} = 1.50 kΩ is selected.

Error Amplifier Compensation

While current mode control typically only requires Type II compensation, it is desirable to layout for Type III compensation to increase flexibility during design and development.

Current mode control boost converters have higher gain with higher output impedance, so it is necessary to calculate the control loop gain at the maximum output impedance, estimated by Equation 57.

$$R_{OUT(max)} = \frac{V_{OUT}}{I_{OUT(min)}} = \frac{24\,V}{0.1A} = 240\,\Omega \quad (57)$$

The transconductance of the TPS40210 current mode control can be estimated by Equation 58.

$$g_M = \frac{0.13 \times \sqrt{L \times \frac{f_{SW}}{R_{OUT}}}}{(R_{ISNS})^2 \times (120 \times R_{ISNS} + L \times f_{SW})} = \frac{0.13 \times \sqrt{10\,\mu H \times \frac{600\,kHz}{240\,\Omega}}}{(12m\Omega)^2 \times (120 \times 12m\Omega + 10\,\mu H \times 600\,kHz)} = 19.1\,A/V \quad (58)$$

The maximum output impedance Z_{OUT}, can be estimated by Equation 59.

$$|Z_{OUT}(f)| = R_{OUT} \times \sqrt{\frac{\left(1 + (2\pi \times f \times R_{ESR} \times C_{OUT})^2\right)}{1 + \left((R_{OUT})^2 + 2 \times R_{OUT} \times R_{ESR} + (R_{ESR})^2\right) \times (2\pi \times f \times C_{OUT})^2}} \quad (59)$$

$$|Z_{OUT}(f_{CO})| = 240\,\Omega \times \sqrt{\frac{\left(1 + (2\pi \times 20\,kHz \times 60\,m\Omega \times 39.8\,\mu F)^2\right)}{1 + \left((240\,\Omega)^2 + 2 \times 240\,\Omega \times 60\,m\Omega + (60\,m\Omega)^2\right) \times (2\pi \times 20\,kHz \times 39.8\,\mu F)^2}} = 0.146\,\Omega \quad (60)$$

The modulator gain at the desired cross-over can be estimated by Equation 61.

$$|K_{CO}| = g_M \times |Z_{OUT}(f_{CO})| = 19.1\,A/V \times 0.146\,\Omega = 2.80 \quad (61)$$

The feedback compensation network needs to be designed to provide an inverse gain at the cross-over frequency for unit loop gain. This sets the compensation mid-band gain at a value calculated in Equation 62.

$$K_{COMP} = \frac{1}{|K_{CO}|} = \frac{1}{2.80} = 0.356 \quad (62)$$

To set the mid-band gain of the error amplifier to K_{COMP} use Equation 63.

$$R4 = R7 \times K_{COMP} = \frac{R7}{|K_{CO}|} = \frac{51.1k\Omega}{2.80} = 18.2k\Omega \quad (63)$$

R4 = 18.7 kΩ selected.

Place the zero at 10th the desired cross-over frequency.

$$C2 = \frac{10}{2\pi \times f_L \times R4} = \frac{10}{2\pi \times 30kHz \times 18.7k\Omega} = 2837pF \quad (64)$$

C2 = 2200 pF selected.

Place a high-frequency pole at about 5 times the desired cross-over frequency and less than one-half the unity gain bandwidth of the error amplifier:

$$C4 \approx \frac{1}{10\pi \times f_L \times R4} = \frac{1}{10\pi \times 30kHz \times 18.7k\Omega} = 56.74pF \quad (65)$$

$$C4 > \frac{1}{\pi \times GBW \times R4} = \frac{1}{\pi \times 1.5MHz \times 18.7k\Omega} = 11.35pF \quad (66)$$

C4 = 47 pF selected.

R-C Oscillator

The R-C oscillator calculation is given as shown in Equation 5, in the datasheet substituting 100 for C_T and 600 for f_{SW}. For a 600-kHz switching frequency, a 100-pF capacitor is selected and a 262-kΩ resistor is calculated (261 kΩ selected)

Soft-Start Capacitor

Since VDD > 8V, the soft-start capacitor is selected by using Equation 67 to calculate the value.

$$C_{SS} = 20 \times T_{SS} \times 10^{-6} \quad (67)$$

For T_{SS} = 12 ms, C_{SS} = 240 nF, a 220-nF capacitor selected.

Regulator Bypass

A regulator bypass capacitor of 1.0-µF is selected per the datasheet recommendation.

TEST DATA

GAIN AND PHASE
vs
FREQUENCY

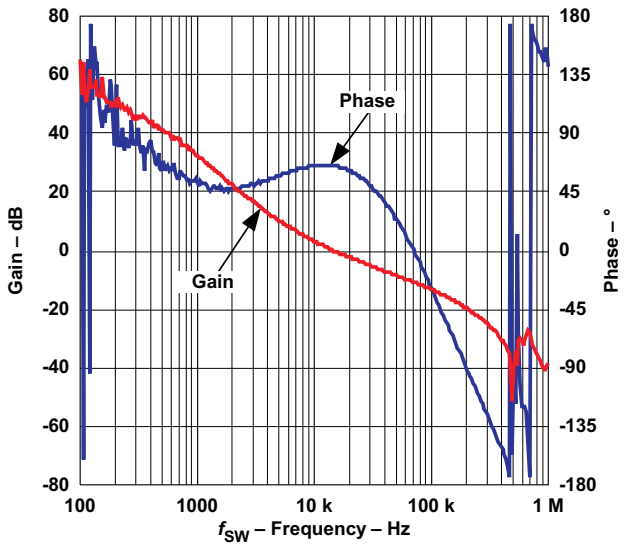


Figure 31.

FET VDS and VGS VOLTAGES
vs
TIME

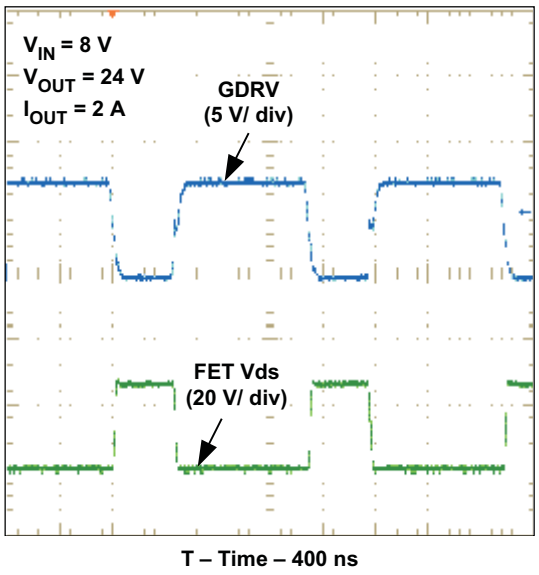


Figure 32.

EFFICIENCY
vs
LOAD CURRENT

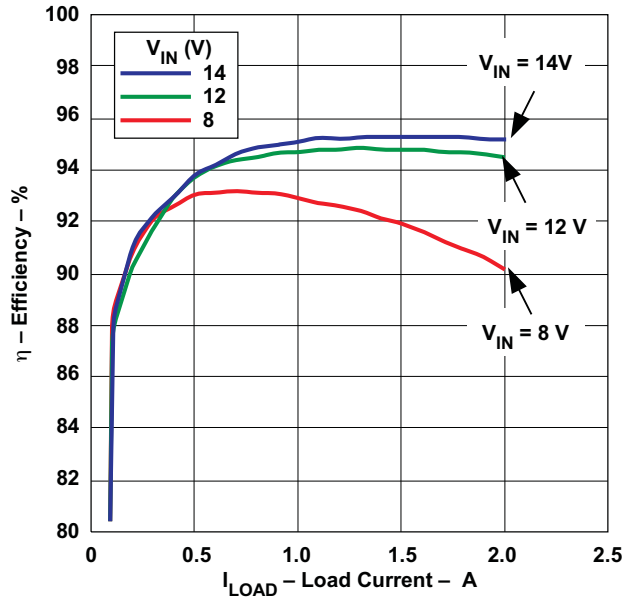


Figure 33.

POWER LOSS
vs
LOAD CURRENT

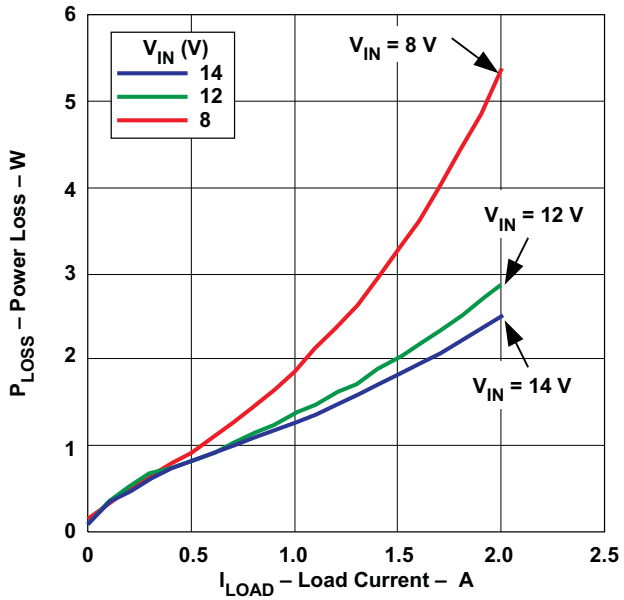


Figure 34.

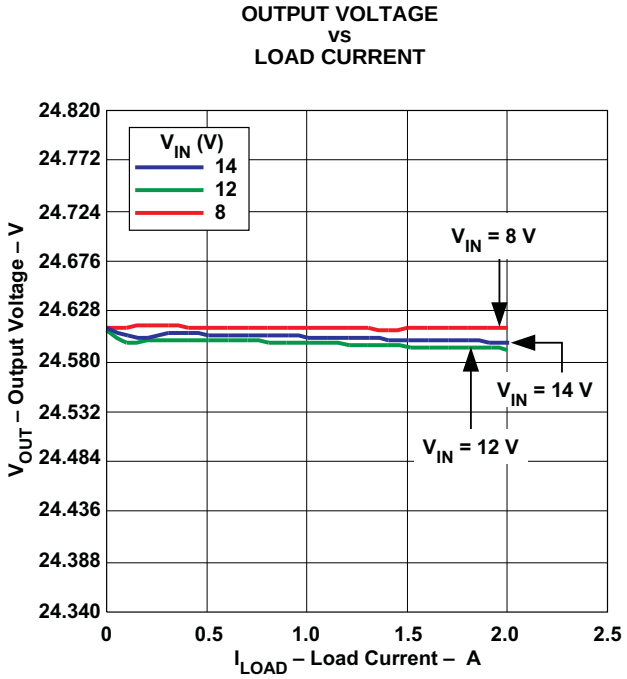


Figure 35.

List of Materials

List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SIZE	PART NUMBER	MANUFACTURER
C1	100 µF, aluminum capacitor, SM, ± 20%, 35 V	0.406 x 0.457	EEEFC1V101P	Panasonic
C2	2200 pF, ceramic capacitor, 25 V, X7R, 20%	0603	Std	Std
C3	100 pF, ceramic capacitor, 16 V, C0G, 10%	0603	Std	Std
C4	47 pF, ceramic capacitor, 16V, X7R, 20%	0603	Std	Std
C5	0.22 µF, ceramic capacitor, 16 V, X7R, 20%	0603	Std	Std
C7	1.0 µF, ceramic capacitor, 16 V, X5R, 20%	0603	Std	Std
C8	10 µF, ceramic capacitor, 25 V, X7R, 20%	0805	C3225X7R1E106M	TDK
C9	0.1 µF, ceramic capacitor, 50 V, X7R, 20%	0603	Std	Std
C10	100 pF, ceramic capacitor, 16 V, X7R, 20%	0603	Std	Std
D1	Schottky diode, 3 A, 40 V	SMC	MBRS340T3	On Semi
L1	10 µH, inductor, SMT, 7.5 A, 12.4 mΩ	0.325 x 0.318 inch	RLF12560T-100M-7R5	TDK
Q1	MOSFET, N-channel, 40 V, 14 A, 9mΩ	SO-8	Si4840DY	Vishay
R3	10 kΩ, chip resistor, 1/16 W, 5%	0603	Std	Std
R4	18.7 kΩ, chip resistor, 1/16 W, 1%	0603	Std	Std
R5	1.5 kΩ, chip resistor, 1/16 W, 1%	0603	Std	Std
R6	261 kΩ, chip resistor, 1/16 W, 1%	0603	Std	Std
R7	51.1 kΩ, chip resistor, 1/16 W, 1%	0603	Std	Std
R9	3.3 Ω, chip resistor, 1/16 W, 5%	0603	Std	Std
R10	1.0 kΩ, chip resistor, 1/16 W, 5%	0603	Std	Std
R11	10 mΩ, chip resistor, 1/2 W, 2%	1812	Std	Std
U1	IC, 4.5 V-52 V I/P, current mode boost controller	DGQ10	TPS40210DGQ	TI

DESIGN EXAMPLE 2

12-V Input, 700-mA LED Driver, Up to 35-V LED String

Application Schematic

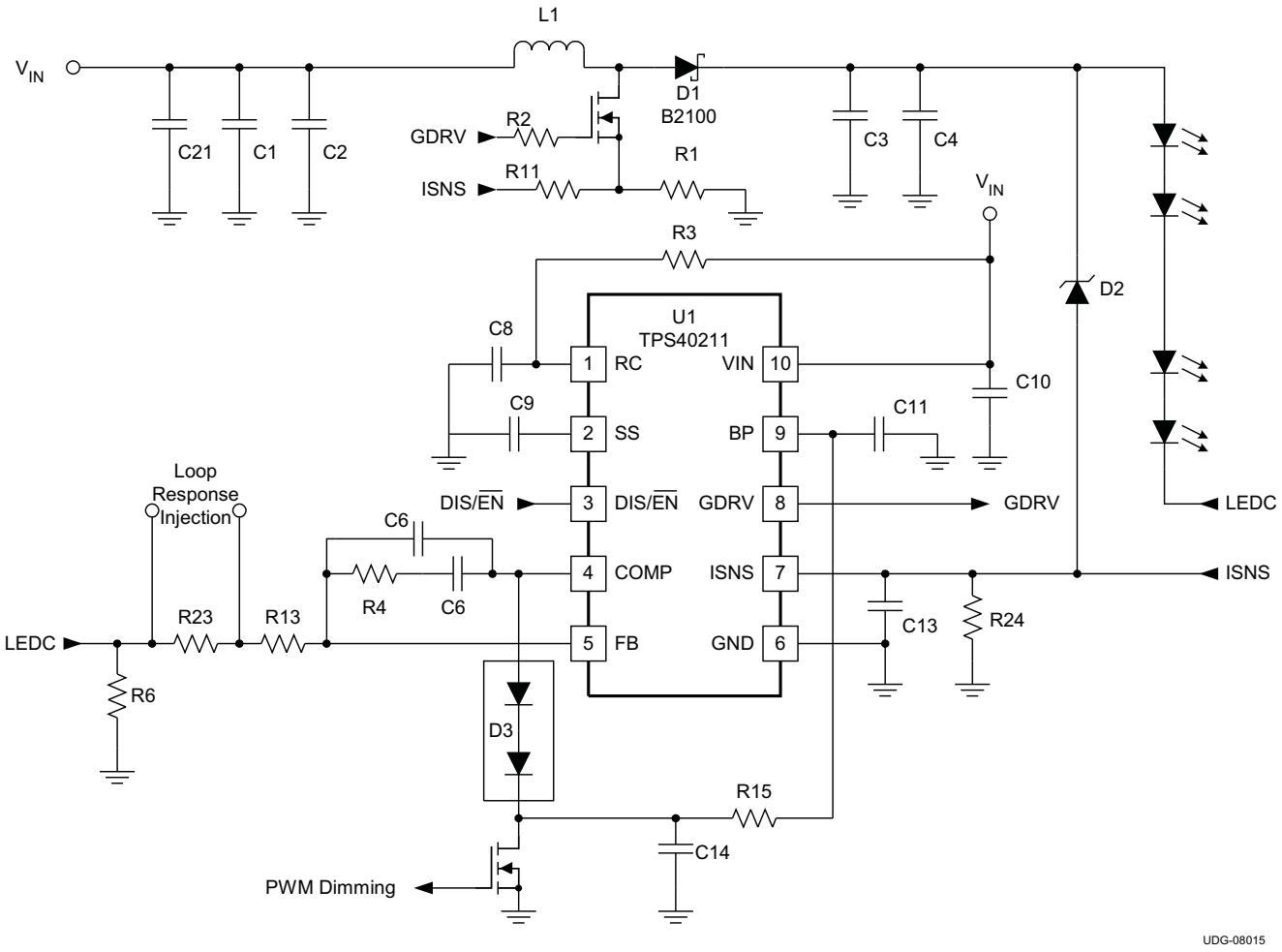


Figure 36. 12-V Input, 700-mA LED Driver, Up to 35-V LED String

List of Materials

List of Materials

REFERENCE DESIGNATOR	TYPE	DESCRIPTION	SIZE
C1,C2	Capacitor	10 µF, 25 V	1206
C3, C4		2.2 µF, 100 V	1210
C5		1 nF, NPO	0603
C6		100 pF, NPO	0603
C8		100 pF	0603
C9		0.1 µF	0603
C10		0.1 µF, 25 V	0805
C11		1 µF, 25 V	1206
C13		220 pF	0603
C14		10 nF, X7R	0603
C21		330µF, 25V electrolytic	
D1	Diode	B2100, SHTKY, 100 V, 2 A	SMB
D2		BZT52C43	SOD-123
D3		MMBD7000	SOT-23
L1	Inductor	Wurth 7447709100, 10 µH, 6 A	12 × 12 × 10 mm
Q1	MOSFET	Si7850DP, 60 V, 31 mΩ	SO-8
Q3		2N7002, 60 V, 0.1 A	SOT-23
R1	Resistor	15 mΩ	2512
R2		3.01 Ω	0805
R3		402 kΩ	0603
R4		14.3 kΩ	0603
R6		0.36 Ω	2512
R11		1 kΩ	0603
R13		30.1 kΩ	0603
R15		49.9 kΩ	0603
R24		10 kΩ	0603
R23		10 Ω	0603
U1	Integrated circuit	TPS40211	DRC-10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS40210DGQ	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS40210DGQG4	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS40210DGQR	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS40210DGQRG4	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS40210DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40210DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40210DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40210DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40211DGQ	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS40211DGQG4	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS40211DGQR	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS40211DGQRG4	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS40211DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40211DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40211DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS40211DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

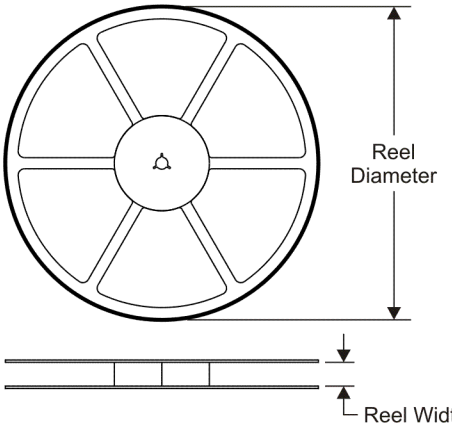
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF TPS40210, TPS40211 :
- Automotive: TPS40210-Q1, TPS40211-Q1

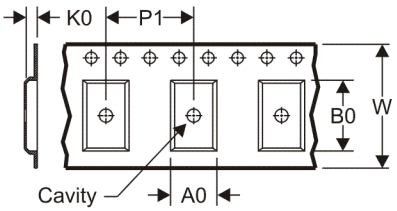
NOTE: Qualified Version Definitions:
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

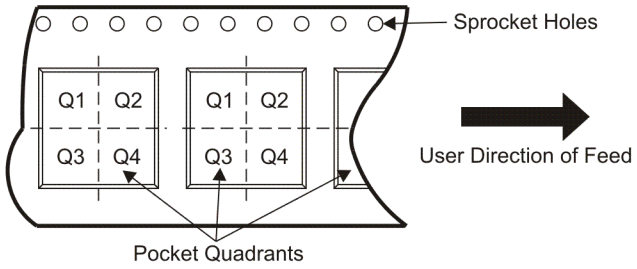


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

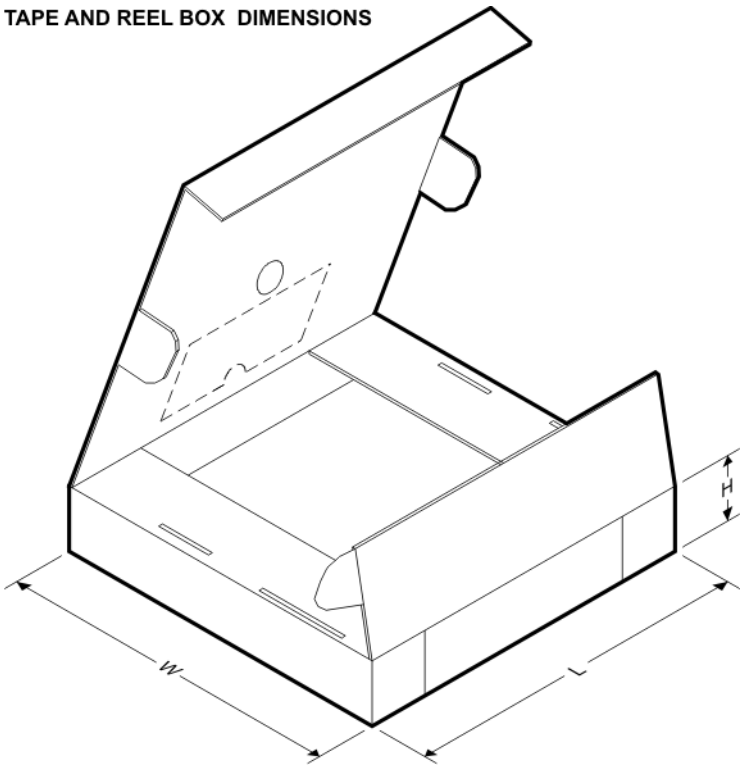
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40210DGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40210DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40210DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40211DGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40211DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40211DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

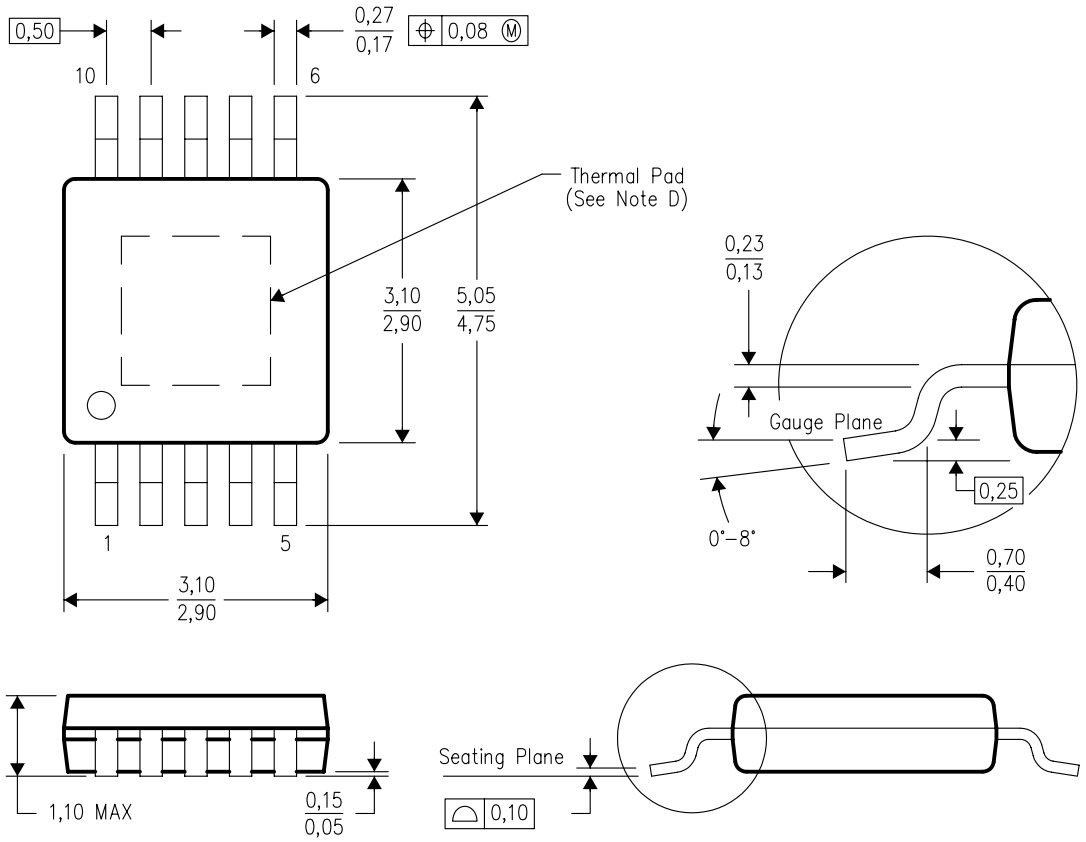
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40210DGQR	MSOP-PowerPAD	DGQ	10	2500	370.0	355.0	55.0
TPS40210DRCR	SON	DRC	10	3000	346.0	346.0	29.0
TPS40210DRCT	SON	DRC	10	250	190.5	212.7	31.8
TPS40211DGQR	MSOP-PowerPAD	DGQ	10	2500	370.0	355.0	55.0
TPS40211DRCR	SON	DRC	10	3000	346.0	346.0	29.0
TPS40211DRCT	SON	DRC	10	250	190.5	212.7	31.8

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



4073273/D 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187 variation BA–T.

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

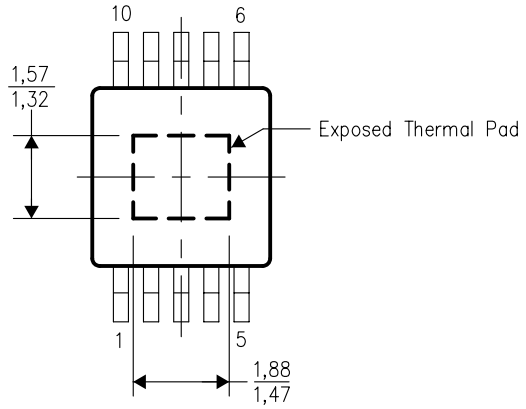
DGQ (S–PDSO–G10)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

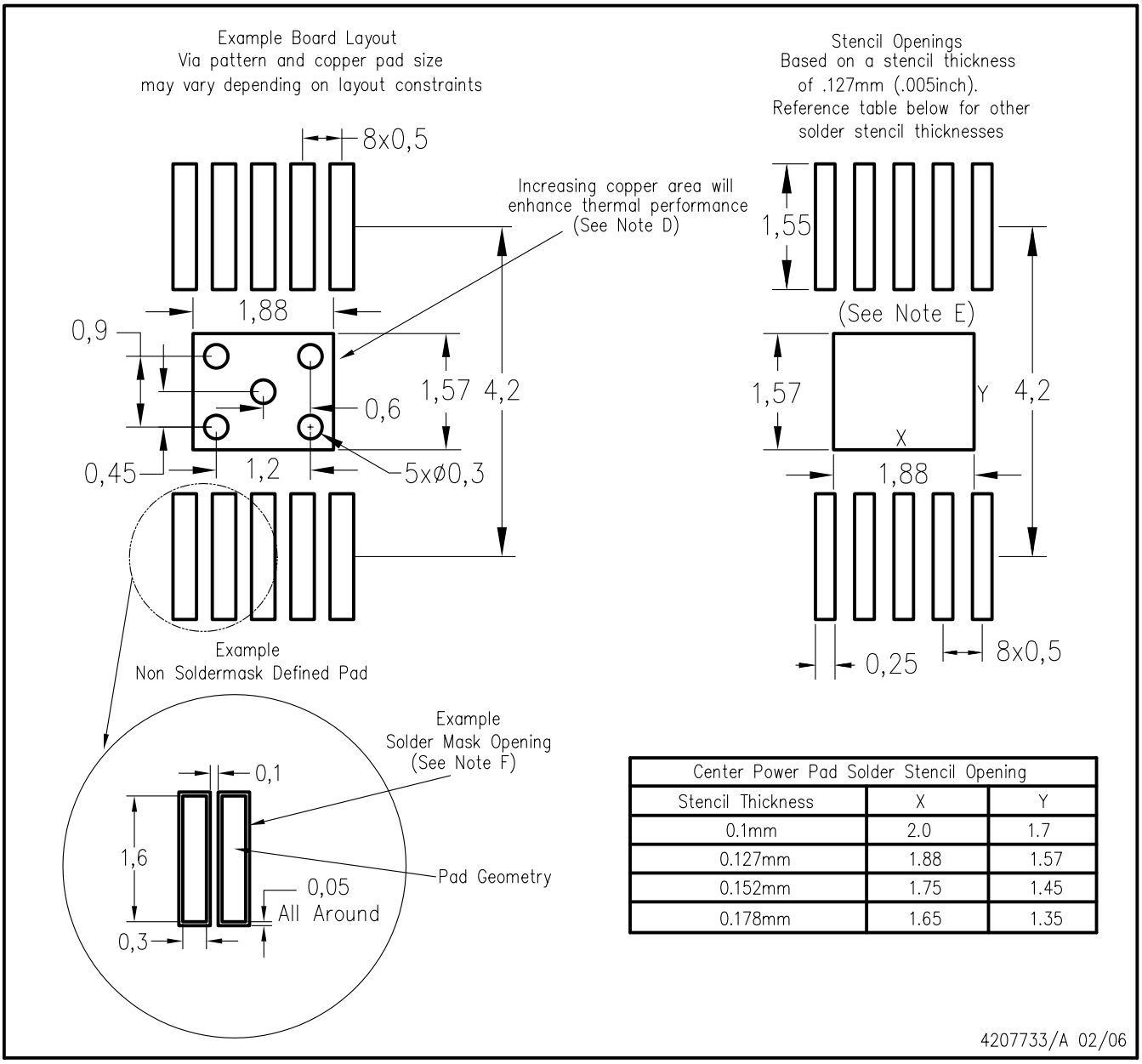


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

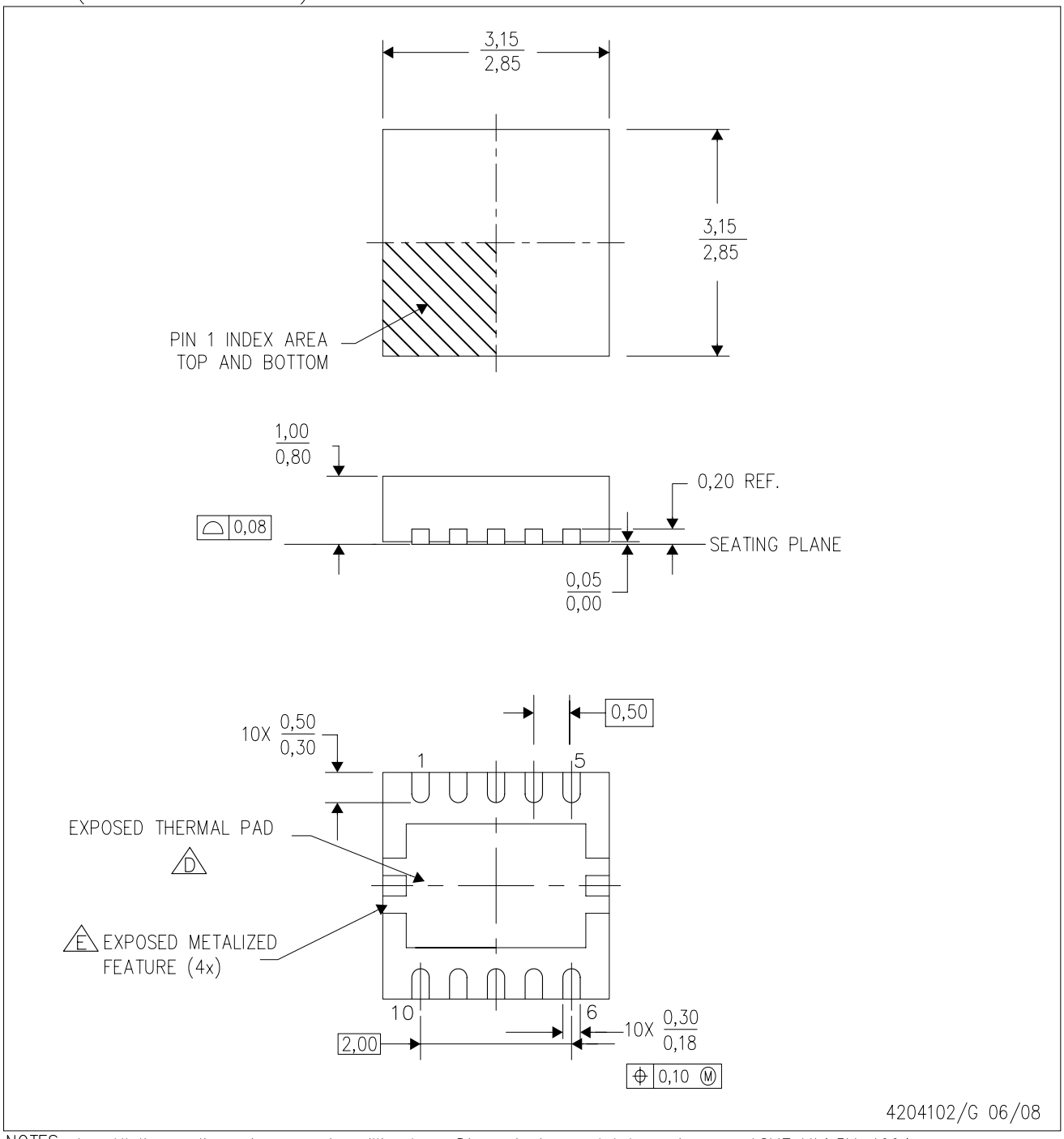
DGQ (R–PDSO–G10) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.88	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

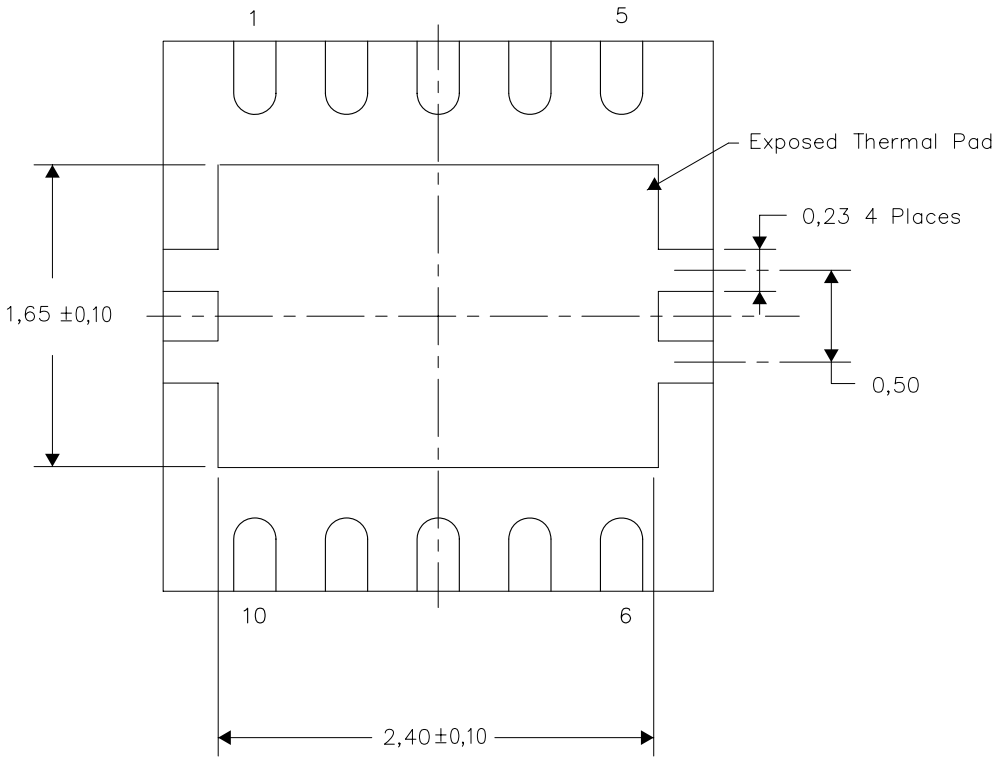
DRC (S–PVSON–N10)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

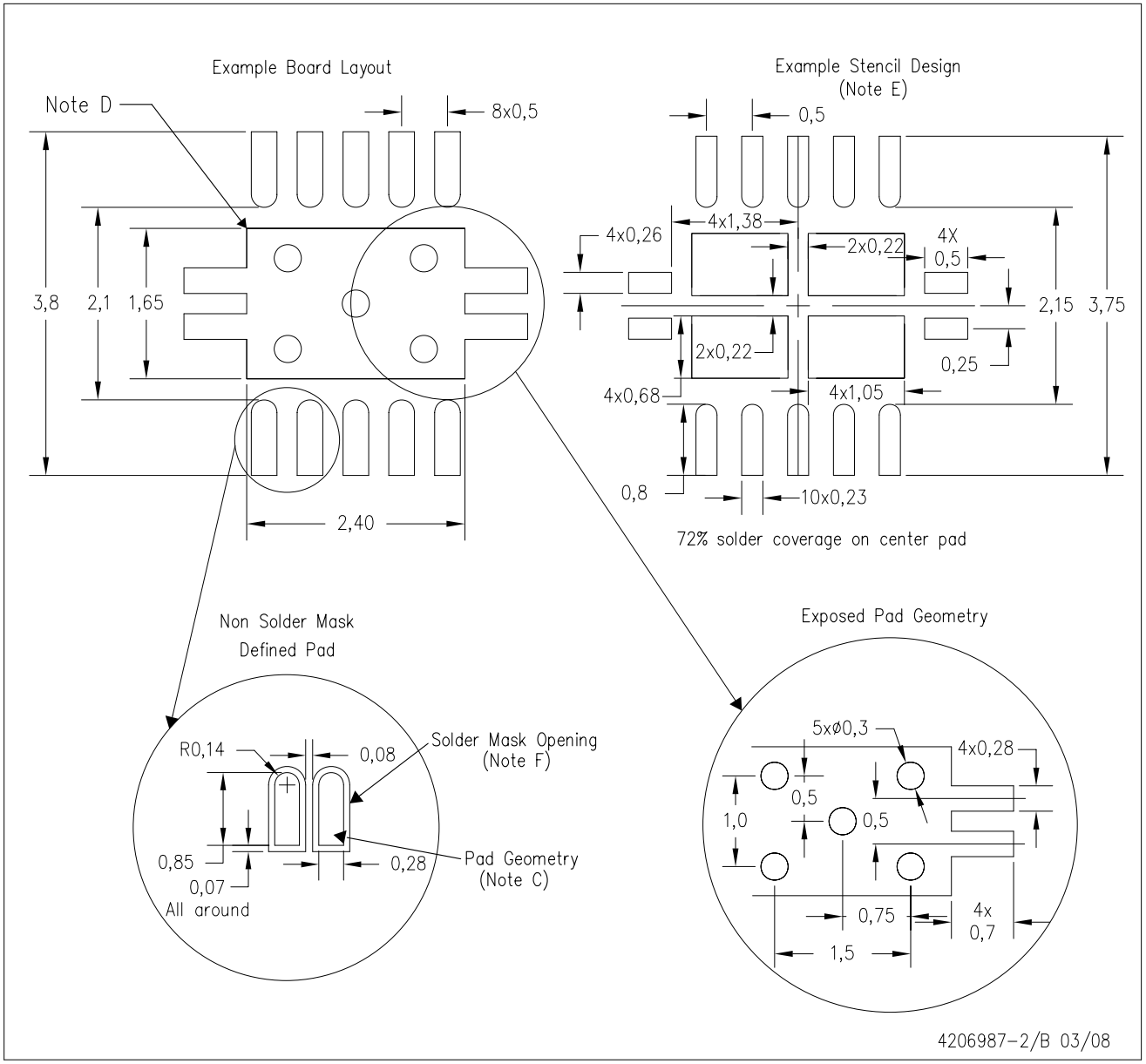


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRC (S–PVSON–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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